Systronix Rev2 JStik Native Execution Java Network Controller Quick Reference

The most commonly used jumpers and I/O connections are shown here. Note that all JStik jumpers and connectors are 2mm. Do not attempt to use larger 0.100 inch connectors or jumpers. For more I/O details, please refer to the JStik and JStik Development Station schematics and sample code. The latest version is available at http://www.jstik.com. Tutorials are on line at http://www.jstik.com. **Be sure to check the website before using JStik for the first time as it may contain essential, last-minute news, documentation, and files.**

HIGH SPEED I/O BUS 15x2 2mm HEADER P2

Buffered high speed I/O bus with 8 bits of data, 12 address lines, 2 chip selects, and read and write strobes. See Notes for mating connector part numbers.

SERIAL A P4

RS-232 serial, if GPIOB1 is Low. Use only a Systronix 2mm DCE or DTE adapter. See Notes.

SERIAL B P5

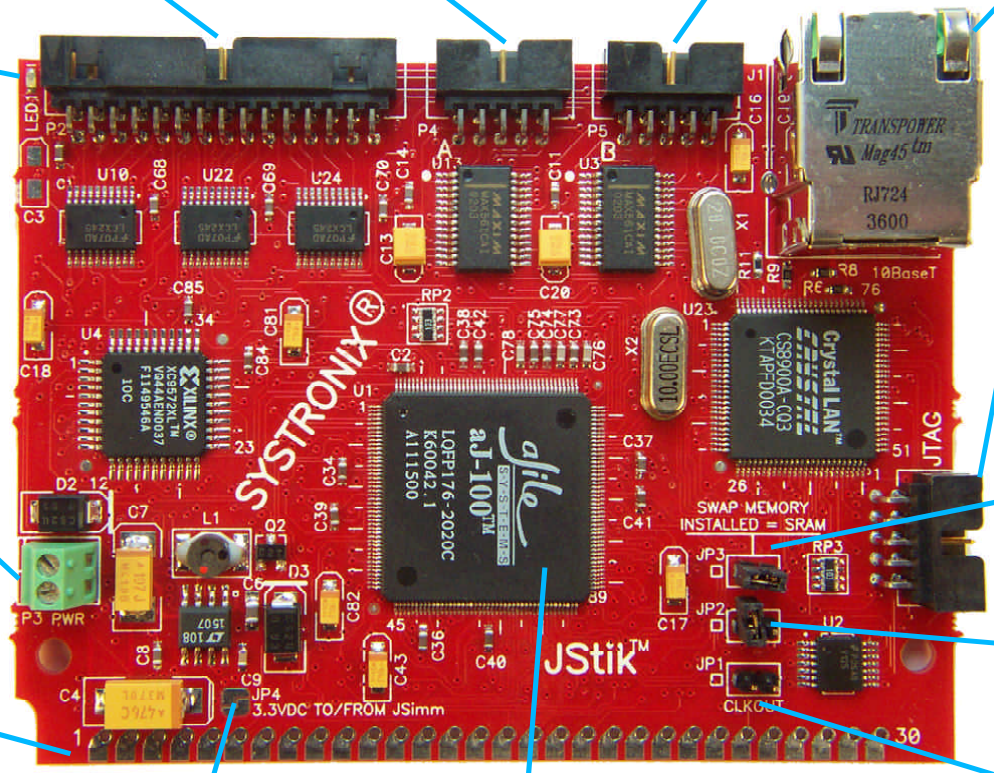
RS-232 serial, if GPIOB2 is Low. Use only a Systronix 2mm DCE or DTE adapter. See Notes.

10BaseT RJ45 J1 & LEDs

Ethernet connection, 10 MBit. Use straight ethernet cable to a hub, or crossover cable to a PC or another JStik. Link LED is on the right; activity LED on the left.

LED1

Red LED, driven by aJ-100 IOB7, buffered. On while aJ-100 is reset, and until changed by your program. Drive GPIOB7 low to turn the LED off.



JTAG PORT P1

Used to program and debug JStamp. connect only to Systronix JTAG adapter or Xilinx Parallel III

OPTIONAL POWER INPUT TERMINAL P3

5-14 VDC regulated or unregulated, upper pin is +. Same as JSimm Pin 7(Vdd which is 5V +/- 5%). Use these terminals if you are not powering JStik from a backplane.

SWAP MEMORY JP3

Selects SRAM or Flash at boot address 0. Installed to boot from SRAM. Remove to program and execute from FLASH

JTAG JUMPER JP2

Must be off to enable JTAG access to the aJ-100. Used only during manufacturing to program the JStik control CPLD.

JSimm EXPANSION

SIMM30 JSimm expansion edge connector. Also compatible with many SimmStick devices. Check each device for compatability!

3.3V PASTE JUMPER JP4

Default: open (no solder)
Add a blob of solder to enable JStik to supply regulated 3.3V at up to 100 mA on JSimm Pin 5

aJile aJ-100

32-bit native Java execution controller with 32-bit wide external data path. Runs at up to 100 MHz.

CLKOUT JUMPER JP1

Default: off
Install to enable a buffered version of the aJ-100 CLKOUT signal on JSimm Pin 6. Caution: CLKOUT is used in the CPLD, so do not change its value.

Top Side

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SERIAL B CTS Paste Jumper JP6

default: open (not present)
Paste jumper which enables GPIOD2 as CTS for serial B. See Notes.

SERIAL A CTS Paste Jumper JP5

default: open (not present)
Paste jumper which enables GPIOD6 as CTS for serial A. See Notes.

PCB Revision Code

This is the revision level of the JStik circuit board (Rev 2).

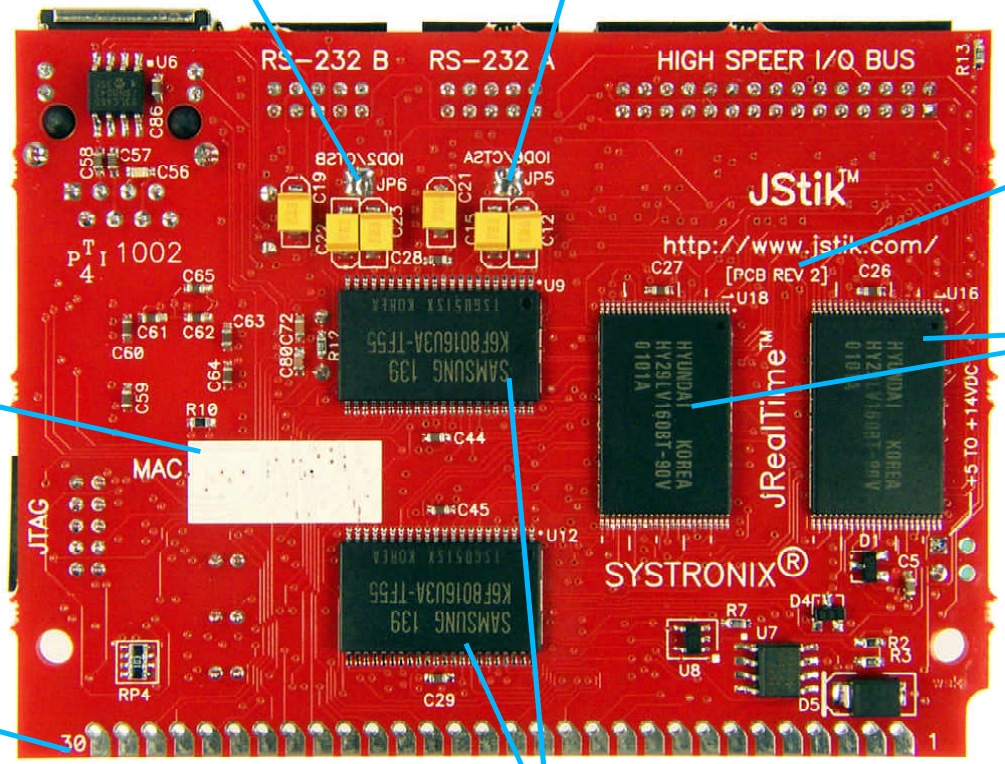
MAC Address Value

The lower four hexadecimal digits of JStik's ethernet MAC are written here. This doubles as the board's serial number.

The entire hexadecimal ethernet MAC address is 00-0B-1B-00-XX-XX where XX-XX are the two octets written here.

Flash

4 MBytes of 90 nsec flash



JSimm EXPANSION

SIMM30 JSimm expansion edge connector. Also compatible with many SimmStick devices. Check each device for compatability!

SRAM

1MB of 10 nsec high speed or
2MB of 55 nsec low power SRAM

Bottom Side

Quick Reference Notes

Install aJile/Systronix tools from CDROM - install JemBuilder and Charade from the CDROM provided with your development kit. Check the website at http://www.jstik.com for the latest configuration files, tips or software. You must use the Systronix version of the aJile tools. Other vendor versions will not have the proper configurations for Systronix products.

SWAP Memory Jumper - important! - JP3 selects whether JStik boots up from SRAM (jumper installed) or flash (jumper not installed). You must build (in JemBuilder) for either SRAM or flash, and set the jumper to match. For program debugging with breakpoints during development, load into SRAM. (Programs in SRAM are lost when power is removed.) Remove this jumper to enable programming FLASH memory, which persists without system power.

Be sure to build, link, and connect for the correct device - you must specify "JStik Configuration" (either RAM or Flash, as appropriate) in JemBuilder, and "aJ100" or "JStik" in Charade in order to correctly build and download programs to JStik. Other JemBuilder configurations may appear to work but will not execute reliably, so use the correct JStik configurations.

JTAG Port - used for loading programs and debugging. Use only the Systronix JTAG adapter and 5x2 100-mil cable, or the Xilinx Parallel III cable. Any other connection voids your warranty and may damage JStik.

Power Supply JStik has an onboard 3.3V converter which uses 5-14 VDC as its input, or you can provide 3.3 VDC yourself. Therefore, power input can be either 5-14 volts DC +/- 10% unregulated or regulated, OR 3.3 VDC +/- 5% regulated.

When powered from a JSimm or SimmStick backplane, JStik normally uses the backplane's 5 VDC power on JSimm bus pin 7. JStik can then supply 3.3 VDC at 100 mA to the backplane (JSimm pin 5) for use elsewhere in your system (if jumper JP4 is closed).

If you are using JStik without a backplane, you can supply 5-14 VDC to the provided screw terminals. The terminal closest to the JSimm connector is negative.

JStik can be powered with 3.3 VDC +/- 5% on JSimm pin 5, if JP4 is closed AND you are not providing any other power input (through the screw terminals or JSimm pin 7)

Serial A RS232 and Serial B RS232, require a Systronix 2mm serial adapter, either DCE or DTE. Use the DTE adapter and a straight-through serial cable to connect to a DCE device such as a modem or LCD. Use the DCE adapter and a straight-through serial cable to connect to a DTE device such as a PC. Use one DCE and one DTE plugged together for a serial loopback test. These headers mate with 2mm IDC receptacles Systronix 2249, DigiKey AKA10K-ND, or AMP 111623-1.

By default serial port RS232 level shifters are disabled. This is to permit driving TTL-level serial devices on the JSimm bus. If you wish to use JStik Serial A or Serial B as RS232 on P4 and P5 you must enable the on-board level shifters. Serial A RS232 level shifters are enabled by driving GPIOB1 low. Serial B RS232 level shifters are enabled by driving GPIOB2 low.

JSimm and SimmStick® Expansion JSimm is compatible with many SimmStick® devices. Check each specific SimmStick® device for compatability first! *Some JSimm I/O pins have multiple functions - such as serial I/O - so please refer to the I/O pinout description before selecting pins to connect to your own devices.* Note that the absolute maximum voltage on a 5V tolerant raw JStik input or I/O pin is 6 VDC. Maximum voltage on a JStik output pin is 5 VDC. Higher voltages can permanently damage JStik and will void your warranty.

High Speed I/O Bus This bus header is a 15x2 2mm right-angle connector. It mates with 2mm IDC receptacles Systronix 2256, DigiKey AKA30K-ND or AMP 111623-7. These I/O pins are 3.3V supply, 5V-tolerant, TTL-level compatible. They will drive 5V TTL I/O directly (but will not properly drive 5V CMOS devices). This I/O bus is fully buffered from JStik's onboard address and data bus, so reasonable cable length or loading will not interfere with JStik's internal operation. Refer to the technical reference for detailed timing and interfacing information.

Power LED Driven by JStik's AJ-100 controller pin IOB7. When IOB7 is high, the heartbeat LED is lit. Since all I/O pins float high during reset, this LED will be lit while JStik is receiving a hardware reset.

JStik™ by SYSTRONIX®

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JStik and JSimm Pin Numbering and Signal Description (also see important notes which follow)

JStik/ JSimm # (note 3)	Name	I/O (note 4)	Description
1	IOC0 SCS0(L)	I/O	8 mA sink/source I/O pin, or SPI Slave Chip Select 0 or slave mode select (when JStik is an SPI slave).
2	IOC1 SCS1(L)	I/O	8 mA sink/source I/O pin, or SPI Slave Chip Select1
3	IOC3 SCS3(L)	I/O	8 mA sink/source I/O pin, or SPI Slave Chip Select 3
4	not used	-	Not used by JStik. This is the SimmStick and JSimm VRAW input 7.5V-18 VDC
5	3.3 VDC	PWR I/O	JStik's power converter provides output of 3.3V @ 100 mA on this pin for your use, when you power JStik's 5-14 VDC input (pin7). Or you can drive this pin with regulated 3.3 VDC +/- 5%. (note 2). Jumper JP4 must be closed to enable 3.3V input or output on this pin .This pin is SimmStick bus ClkIn/A4, is not used on many SimmStick products, and SimmStick does not have a 3.3V pin, so we chose it for 3.3V on the JSimm bus and it will typically have no conflict on SimmStick systems.
6	CLKO	O	Clkout signal, a programmable divider output. Enabled by jumper JP1. Buffered from the aJ-100.
7	5 VDC	PWR I	The JSimm or SimmStick bus provides a fixed 5VDC on this pin. JStik can actually be powered by a wider range of 5-14 VDC on this pin, but the SimmStick and JSimm specifications make this pin fixed 5 VDC. See note 2 for more details.
8	CRST(L)	I/O	Open-drain reset to/from JStik. Use this signal to reset JStik from external logic or to reset your external logic when JStik resets. There is no reset pushbutton on JStik.
9	GND	PWR	GND
10	IOB4	I/O	8 mA sink/source I/O pin. Can be CS4 but not used as such on JStik.
11	IOB5	I/O	8 mA sink/source I/O pin. Can be CS5 but not used as such on JStik.
12	IOD5 RXDA	I/O	8 mA sink/source I/O pin, or UARTA RXD (On the JSimm bus this signal is TTL level- not RS232 level - note 1)
13	IOD4 TXDA	I/O	8 mA sink/source I/O pin, or UARTA TXD (On the JSimm bus this signal is TTL- not RS232 level - note 1)
14	IOC2 SCS2(L)	I/O	8 mA sink/source I/O pin, or SPI Slave Chip Select 2
15	IOA0 IOE0	I/O	IOA0: 24 mA sink/source I/O pin. IOE0: 8 mA sink/source I/O pin, or Timer/Counter 2 input control/output B.
16	IOA1 IOE2	I/O	IOA1: 24 mA sink/source I/O pin. IOE2: 8 mA sink/source I/O pin, or Timer/Counter 2 external clock input
17	IOA2 IOE5	I/O	IOA2: 24 mA sink/source I/O pin IOE5: 8 mA sink/source I/O pin, or Timer/Counter 1 external clock input
18	IOA3 TCLK0	I/O	IOA3: 24 mA sink/source I/O pin TCLK0: optional external clock input for Timer/Counter 0 or the aJ100 prescaler block
19	IOA4 IOE1	I/O	IOA4: 24 mA sink/source I/O pin IOE1: 8 mA sink/source I/O pin, or Timer/Counter 2 input control/output A
20	IOC4 SPIMOSI	I/O	8 mA sink/source I/O pin. Also functions as SPI MOSI when in SPI master mode and MISO when a SPI slave.
21	IOC5 SPIMISO	I/O	8 mA sink/source I/O pin. Also functions as SPI MISO when in SPI master mode and MOSI when a SPI slave.
22	IOC6 SPICLK	I/O	8 mA sink/source I/O pin. Also SPI Transfer Clock.
23	IOA5 IOE3	I/O	IOA5: 24 mA sink/source I/O pin and GPIOE 8 mA sink/source I/O pin IOE3: 8 mA sink/source I/O pin or Timer/Counter 1 Input Control/Output B
24	IOA6 IOE4	I/O	IOA6: 24 mA sink/source I/O pin and GPIOE 8 mA sink/source I/O pin IOE4: 8 mA sink/source I/O pin or Timer/Counter 1 Input Control/Output A
25	IOA7 IOE6	I/O	IOA7: 24 mA sink/source I/O pin and GPIOE 8 mA sink/source I/O pin IOE6: 8 mA sink/source I/O pin or Timer/Counter 0 Input Control/Output B
26	IOE7 IOC7	I/O	IOE7: 8 mA sink/source I/O pin or Timer/Counter 0 Input Control/Output A IOC7: 8 mA sink/source I/O pin or UART Receive Clock
27	IOD0 TXDB	I/O	8 mA sink/source I/O pin, or UARTB TXD (TTL- not RS232 level - note 1)
28	IOD1 RXDB	I/O	8 mA sink/source I/O pin, or UARTB RXD (TTL- not RS232 level - note 1)
29	IOD6 CTSA	I/O	8 mA sink/source I/O pin, also can function as CTS for serial A if JP5 is closed
30	N/C	I/O	Dallas 1-Wire on JSimm bus. Not connected to or used by JStik.

Important Notes

Note 1: JStik I/O Pin Voltages and Logic Thresholds - JStik GPIO pins are 3.3V max Voh, compatible with TTL levels, and are 5V I/O tolerant. They interface with no additional circuitry to 3.3V and 5V TTL-level devices. They will not drive 5V CMOS outputs directly.

Note 2: JStik power can be either regulated 3.3 VDC +/- 5%, or unregulated 5-14 VDC +/- 10%. When JStik is plugged into the Systronix JSimm 6-slot backplane, it receives 5 VDC on JSimm pin 7. SimmStick backplanes also provide fixed 5VDC on their pin 7. If you don not use a standard backplane and devise your own, or power this pin via other means, you may provide 5-14 VDC. If you power JStik's JSimm pin 7 then JStik's 3.3V I/O (pin 5) provides output of 3.3V @ 100 mA for your use. If you provide regulated 3.3 VDC on pin 5, do not also apply power to pin 7.
Never apply your own power to both JSimm Pin 5 and JSimm Pin 7.

Note 3: JSimm pins and GPIO Pin Functions - Many aJ-100 GPIO pins are brought out to the JSimm edge connector. Many of these GPIO pins may be individually configured as input or an output, and may also be configured to generate a CPU interrupt. Many GPIO pins have **multiple functions** (IOC6 is also the SPI clock). After a hardware reset such multi-purpose signals are configured as GPIO inputs. Use the com.ajile.drivers.gpio package to control GPIO pins, and see the JStik Technical Reference for more details.

In addition to some individual JStik GPIO pins serving multiple functions, we have further complicated the matter by connecting some JSimm signals to two GPIO pins. We call these **shared GPIO pins**, for lack of a better term. For example, JSimm.15 is the shared combination of GPIOA0 and GPIOE0. There are several logical reasons for JSimm sharing GPIO pins.

First, JStik remains compatible with JStamp in its assignment of GPIO pins to JSimm signals.

Second, it brings out all 8 bits of GPIOA from JStik's aJ-100 controller, giving JSimm a true byte-wide GPIO port. (This is not possible with JStamp's aJ-80 controller). GPIOA is capable of sinking and sourcing 24 mA per pin.

Third, it makes more special function pins available to the JSimm bus. For example, JStik's JSimm.26 is connected to both GPIOE7 and GPIOC7.

These 'shared' GPIO pins don't conflict with each other as long as only one is active as an output at any instant.

Note 4: I/O Direction is from the viewpoint of JStik. That is, an input is a signal received by JStik.

GPIO Pins Used Internal to JStik Other GPIO pins are not available on the JSimm bus but have functions internal to the JStik module. For example, GPIOB7 is the heartbeat LED and is not brought to the JSimm bus. If you wish to drive this LED from your own program, use the GpioPin class - do not write to all of GPIOB as a byte wide port since the other GPIOB bits have their own special uses on JStik, and you don't want to interfere with them.

Systronix provides a JStik API to use in controlling GPIO functions such as serial level shifter enables.

All aJ-100 GPIO Pins as Used on JStik

GPIOA[7..0] - all available on the JSimm bus. Some pins have multiple functions and some are shared with other GPIO pins.

GPIOB7 - JStik heartbeat LED
GPIOB6 - ethernet interrupt. Do not access this bit yourself.
GPIOB5 - JSimm.11
GPIOB4 - JSimm.10
GPIOB3 - Address 27. Do not access this bit yourself.
GPIOB2 - Serial B RS-232 level shifter enable.
GPIOB1 - Serial A RS-232 level shifter enable.
GPIOB0 - Address 24. Do not access this bit yourself.

GPIOC[7..0] - all available on the JSimm bus. Some pins have multiple functions and some are shared with other GPIO pins.

GPIOD7 - RTS Serial A
GPIOD6 - CTS Serial A if JP5 is closed, also JSimm.29
GPIOD5 - RXD Serial A, also JSimm, also JSimm.12
GPIOD4 - TXD Serial A, also JSimm.13
GPIOD3 - RTS Serial B
GPIOD2 - CTS Serial B if JP6 is closed
GPIOD1 - RXD Serial B, also JSimm.28
GPIOD0 - TXD Serial B, also JSimm.27

GPIOE[7..0] - all available on the JSimm bus. Some pins have multiple functions and some are shared with other GPIO pins.

JStik Documentation and Resources

aJ-80 and aJ-100 - both aJile controllers share the same 32-bit CMOS core and differ only in pinout (the aJ-100 is a larger package so brings out more pins). The aJ-80 has an 8-bit external data bus - the aJ-100 has 32-bits. They share the same technical reference, Java edition and profile support, and so forth.

AJ-100 Reference Manual - available online at http://www.ajile.com/aj100.htm as a PDF document. This is the definitive source for information about inner workings of the aJile controllers.

On-line Support Groups: there are JRealTime and JStamp Yahoo user groups at http://groups.yahoo.com/group/jrealtime and /jstamp. Links to these and other third party support and information groups may be found at http://www.jstik.com

Java, J2ME, CLDC, and RealTime Java Information: J2ME and CLDC information and packages are available online from Sun at http://www.sun.com/software/communitysource/j2me/cldc/download.html - also see the website of the book Practical Embedded Java at http://www.PracticalEmbeddedJava.com

JStik in Robotics: www.jcx.systronix.com

JCX is a hardware platform with LEGO®-compatible inputs and outputs, (also usable with other common robotic sensors and actuators). It can be used with JStamp or JStik control modules.

Tutorial & Examples, Educational Use

An ongoing tutorial and sample programs are available on our web site at www.jstampu.com, and at www.PracticalEmbeddedJava.com. There are also links to use of JStamp, JStik and related products in education, particularly university and college programs.

Trademarks

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