

JStik32 – REVISIONS

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SCH REV	PCB REV	DATE	BY	DESCRIPTION	SCH REV	PCB REV	DATE	BY	DESCRIPTION			
0.0		01 OCT 03	wsk	START	2.22	3.0	03 JAN 16	wsk	Sheet 12: EXPANDED NOTE AT P3;			
1.0	1.0	01 NOV 13	wsk	Sheet 2: Added memory map; Sheet 5: Added note;	2.23	3.0	03 JUN 03	wsk	Sheet 8: Expanded notes at the JSimm edge connector; Sheet 12: Further expansion and enhancement of note at P3;			
2.0	2.0	01 DEC 05	wsk	Sheets 3, 5, 6, 7, & 9: Corrected address bus inter-sheet symbols; Sheets 3 & 8: Removed bus IOB[7..0] and intersheet references; Sheets 8, 10, & 12: Changed U2 power net to +3.3VDC;  Sheet 3: Deleted pullup on WAIT(L); Deleted RP1; Connected U1 pins 58 & 61 to RP2 pin 3; Moved ethernet interrupt from IOB3 to IOB6; Added net A27; Moved U2B, LED1, & R13 from sheet 8; Changed LED1 anode voltage to +3.3VDC; Connected U2 pin 4 to U1 pin 107 (IOB7); Renamed nets IOB4/CS4(L) & IOB5/CS5(L) to IOB4 & IOB5; Added JSimm IF intersheet reference;  Sheet 5: Deleted note; Changed U9 & U12 to K6F8016U3A (512 x 16); Added A20; Added Memory Options table;  Sheet 6: Added net A27; Deleted IOB4/CS4(L) & IOB5/CS5; Renamed JP4 to JP3;  Sheet 8: Renamed IOE5 to IOE6; Connected IOA[7..5] to IOE[6,4,3]; Moved U2B, LED1, & R13 to Sheet 3; Renamed IOE7/IrDA_CLK to IOE7; Connected IOE7 to IOC7; Deleted C10, +5VDC net & intersheet references; Renamed JP3 to JP4;  Sheet 9: Corrected buffer control signals U22; Changed U10, U22, & U24 to 74LCX245; Deleted C71, C79, C83; Added C1 & C3;  Sheet 10: Replaced R14 with RP3D; Connected RP3 pins 5 & 6 to 3.3VDC; Sheet 11: Replaced 3 & U13 with ADM561JRS transceivers; Changed C12, C13, C15, & C19 - C23 to 1.0uF Tant.; Added note, JP5, & JP6;  Sheet 12: Corrected intersheet reference for CRST(L); Assigned values to C72 & C80; Added D5, P3;								
2.1	2.0	02 FEB 01	wsk	Sheet 7: Changed R6, R8 to 7R5 1%; Sheet 12: Corrected crystal frequency and inductor value;								
2.11	2.0	02 MAR 11	wsk	Sheet 2: Corrected Ethernet Address map; Sheet 12: Corrected crystal frequency and inductor value;								
2.20	3.0	02 MAR 11	wsk	Sheet 6: Deleted connection to sheet 8; Sheet 8: Deleted connection to sheet 6; Connected U1-122 to net IOE7/IOC7; Changed JP4 note;  Sheet 11: Added Serial port labels;								
2.21	3.0	02 OCT 16	wsk	Sheet 2: Clarified memory map (hopefully);								
2.23		2002 SEP 17	bab	Sheet 11: Corrected serial port labels on P4 and P5								

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8	JSimm INTERFACE
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10	JTAG
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TO DO:

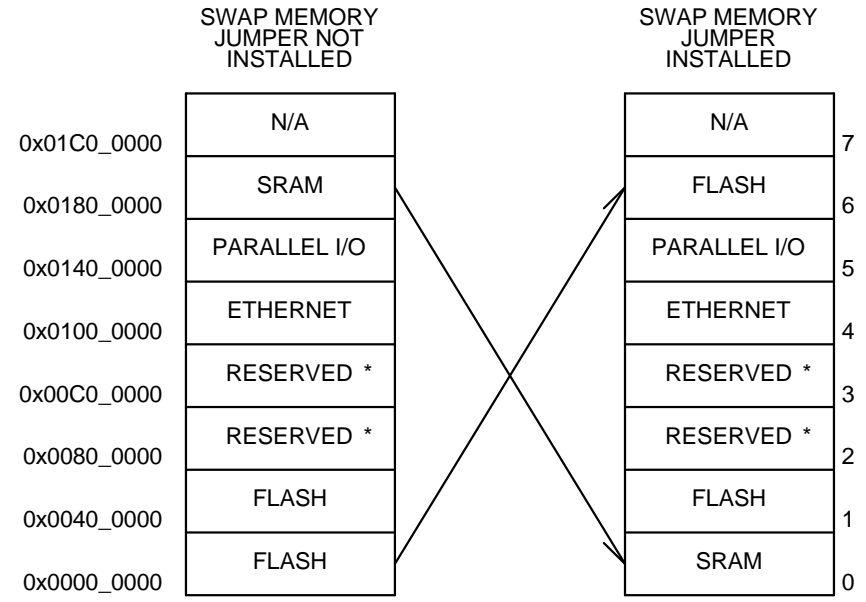
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Title	JStik 32 REVISIONS	
Size	Number	Rev
B		2.23
Date	Wed Sep 17, 2003	Drawn by wsk
Filename	JStik32_223.sch	Sheet 1 of 12

MEMORY MAP – SWAP MEMORY JUMPER NOT INSTALLED

ADDRESSES	DEVICE
0x0000_0000 - 0x00FF_FFFF 0x0000_0000 - 0x003F_FFFF 0x0000_0000 - 0x007F_FFFF 0x0080_0000 - 0x00FF_FFFF	FLASH 16Mb (4MB) ENTIRE DEVICE 32Mb (8MB) ENTIRE DEVICE RESERVED. NO PHYSICAL DEVICES PRESENT; IMAGES POSSIBLE
0x0130_0000 - 0x013F_FFFF 0x0130_0000 - 0x0130_FFFF 0x0131_0000 - 0x0131_FFFF	ETHERNET CONTROLLER MEMORY SPACE I/O SPACE
0x0140_0000 - 0x017F_FFFF 0x0140_0000 - 0x0140_FFFF 0x0141_0000 - 0x0141_FFFF	PARALLEL I/O CHIP SELECT X_CS0(L) CHIP SELECT X_CS1(L)
0x0180_0000 - 0x01BF_FFFF 0x0180_0000 - 0x01BF_FFFF	SRAM 16Mb (2MB)



\* RESERVED FOR FUTURE

JUMPERS			
JUMPER	SHUNT INSTALLED?	DESCRIPTION	SHEET
JP1	YES	ENABLES aJ-100 CLKO SIGNAL ONTO THE JSimm BUS.	12
	NO	ALLOWS ANOTHER SOURCE TO DRIVE THE JSimm BUS SIGNAL CLKO/A5. CLKO/A5 IS NOT USED ON JStik.	
JP2	YES	ROUTES THE JTAG PORT TO THE CPLD (U4). NOT NORMALLY STUFFED.	10
	NO	ROUTES THE JTAG PORT TO THE aJ-100 (U1). NOT NORMALLY STUFFED.	
JP3	YES	BOOT FROM SRAM; SEE MEMORY MAP FOR DETAILS.	6
	NO	BOOT FROM FLASH; SEE MEMORY MAP FOR DETAILS.	
JP4	YES	ALLOWS JStik TO PROVIDE 3.3VDC (100mA MAX) TO THE JSimm BUS. JStik MAY ALSO RECEIVE 3.3VDC +/- 5% FROM THE JSimm BUS.	8
	NO	DEFAULT. JStik DOES NOT RECEIVE OR PROVIDE 3.3VDC FROM/TO THE JSimm BUS.	
JP5	YES	DEFAULT. CTSA CONTROLS IOD6/CTSA WHEN SERIAL A TRANSCEIVER IS ENABLED.	11
	NO	IOD6 CONTROLS IOD6/CTSA WHEN SERIAL A TRANSCEIVER IS ENABLED.	
JP6	YES	DEFAULT. CTSB CONTROLS IOD2/CTSB WHEN SERIAL B TRANSCEIVER IS ENABLED.	11
	NO	IOD2 CONTROLS IOD2/CTSB WHEN SERIAL B TRANSCEIVER IS ENABLED.	

MEMORY MAP – SWAP MEMORY JUMPER INSTALLED

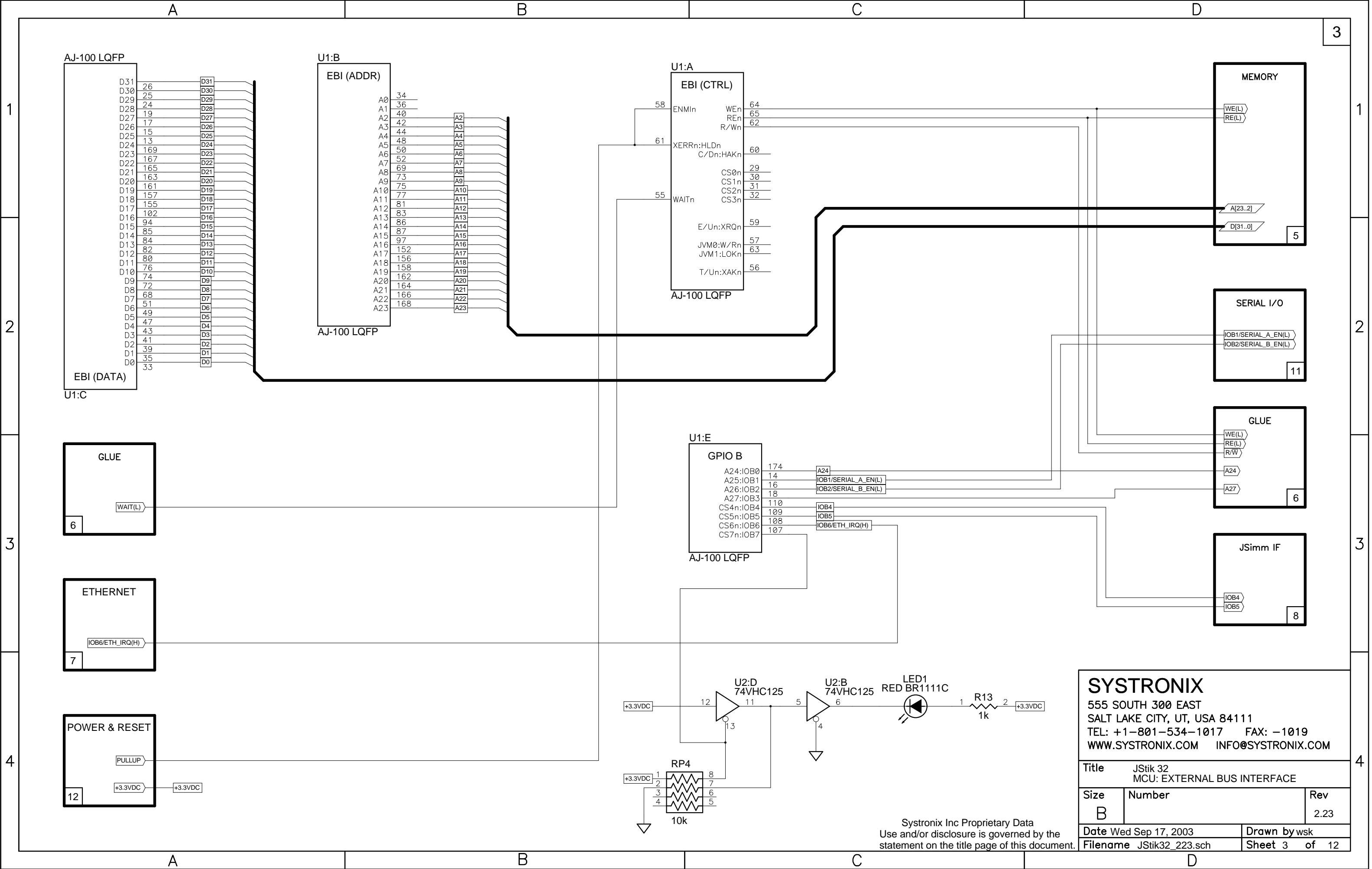
ADDRESSES	DEVICE
0x0000_0000 - 0x003F_FFFF 0x0000_0000 - 0x003F_FFFF	SRAM - NOTE 1 16Mb (2MB) LOW-SPEED (55nS)
0x0040_0000 - 0x00FF_FFFF 0x0040_0000 - 0x007F_FFFF 0x0080_0000 - 0x00FF_FFFF	FLASH 32Mb (8MB) UPPER HALF RESERVED. NO PHYSICAL DEVICES PRESENT; IMAGES POSSIBLE
0x0130_0000 - 0x013F_FFFF 0x0130_0000 - 0x0130_FFFF 0x0131_0000 - 0x0131_FFFF	ETHERNET CONTROLLER MEMORY SPACE I/O SPACE
0x0140_0000 - 0x017F_FFFF 0x0140_0000 - 0x0140_FFFF 0x0141_0000 - 0x0141_FFFF	PARALLEL I/O CHIP SELECT X_CS0(L) CHIP SELECT X_CS1(L)
0x0180_0000 - 0x01BF_FFFF 0x0180_0000 - 0x01BF_FFFF 0x0180_0000 - 0x01BF_FFFF	FLASH 16Mb (4MB) ENTIRE DEVICE 32Mb (8MB) LOWER HALF

- NOTES:  
 1. ADDRESSES IN THE LOW 4MB OUTSIDE THE SRAM PHYSICAL DEVICE ARE NOT AVAILABLE.  
 2. PROGRAMMERS SHOULD NOTE THAT IMAGES OF MEMORY AND I/O WILL APPEAR OUTSIDE OF THE ILLUSTRATED MEMORY MAP. CAVEAT LECTOR.

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Title	JStik 32 NOTES	
Size	Number	Rev
B		2.23
Date	Wed Sep 17, 2003	Drawn by wsk
Filename	JStik32_223.sch	Sheet 2 of 12

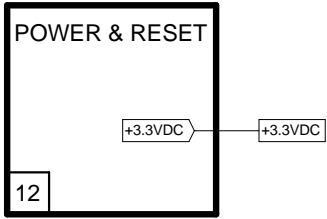
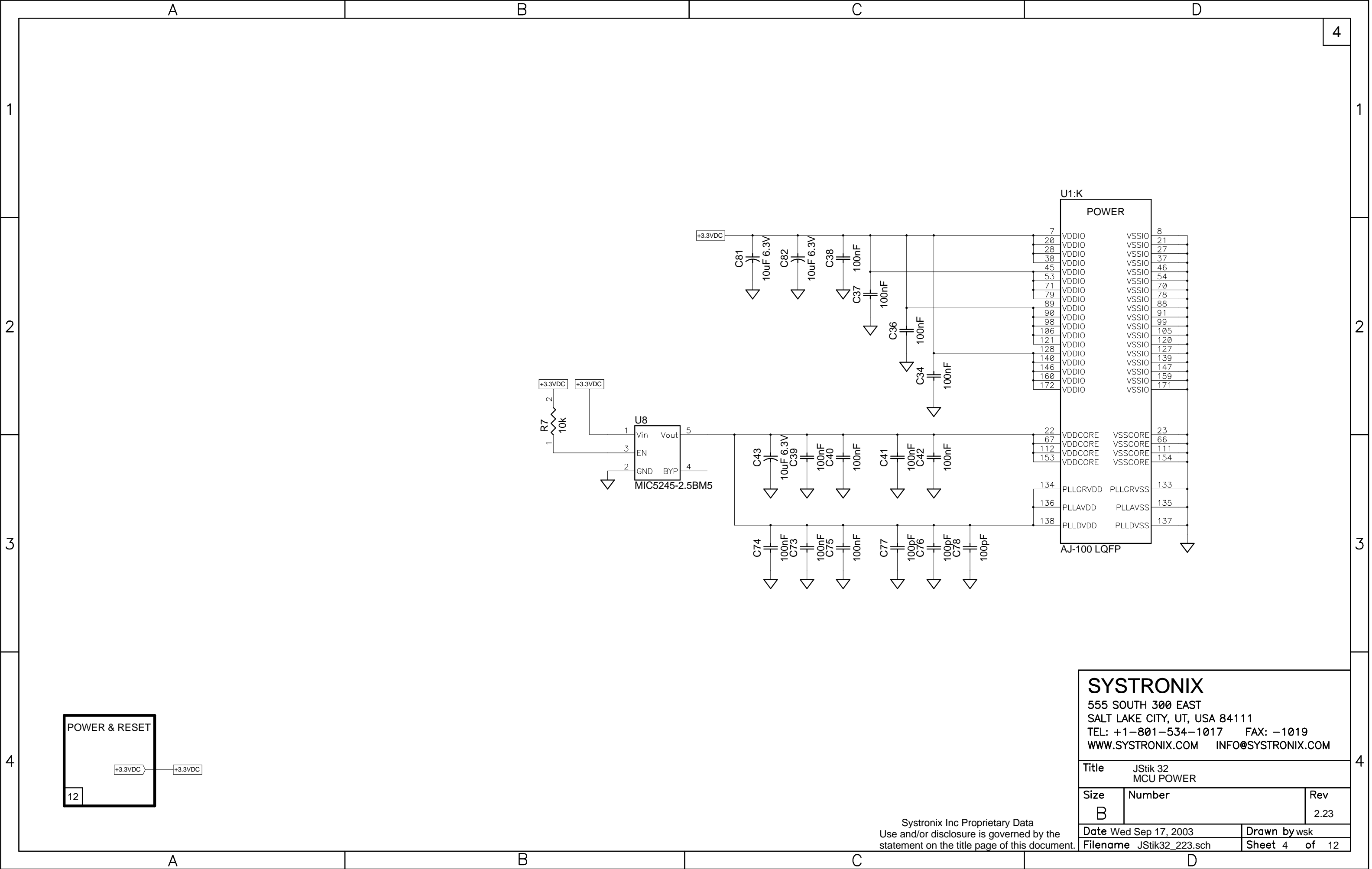
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Title		JStik 32 MCU: EXTERNAL BUS INTERFACE
Size	Number	Rev
B		2.23
Date	Wed Sep 17, 2003	Drawn by wsk
Filename	JStik32_223.sch	Sheet 3 of 12

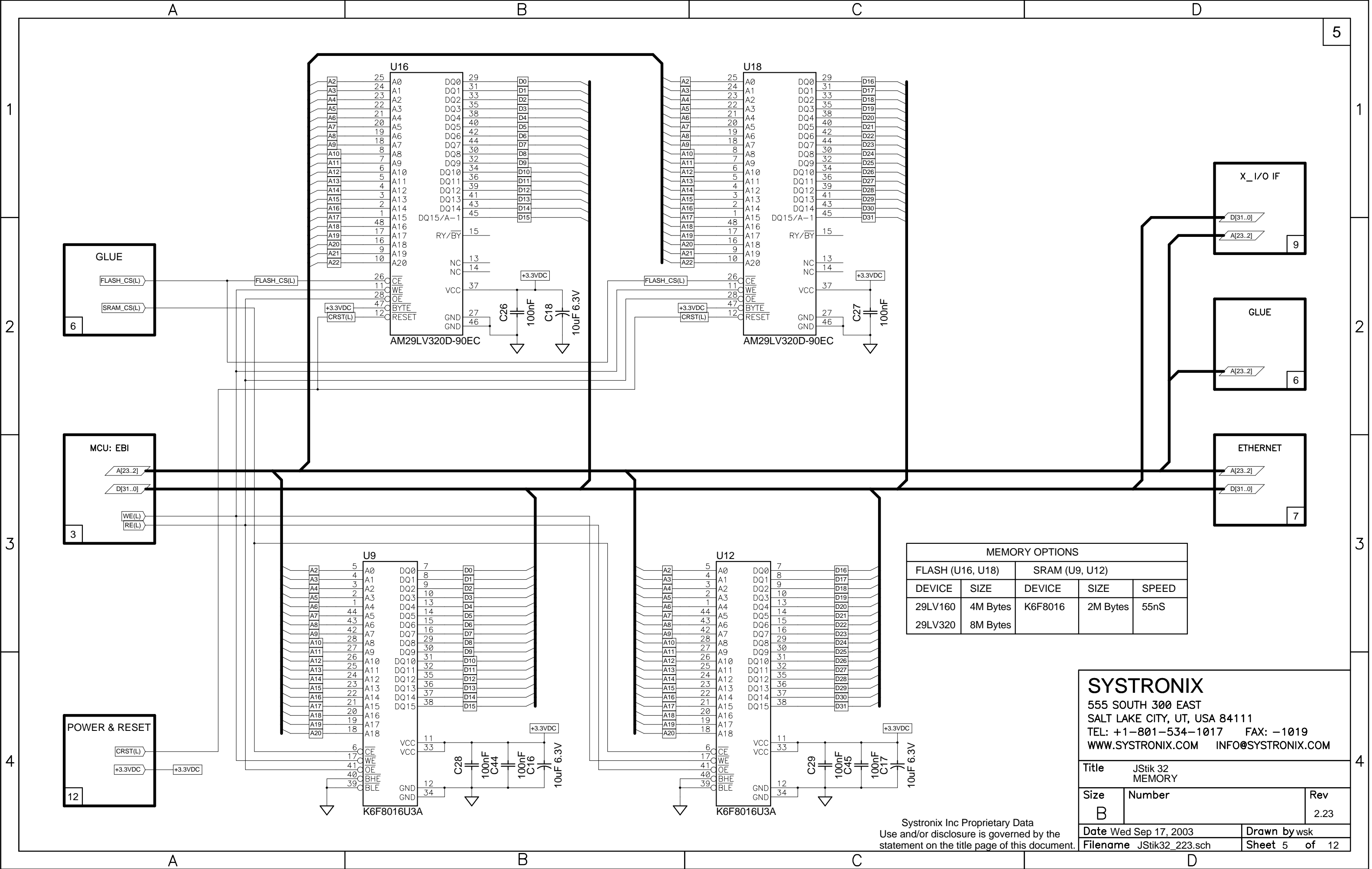
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Title		JStik 32 MCU POWER
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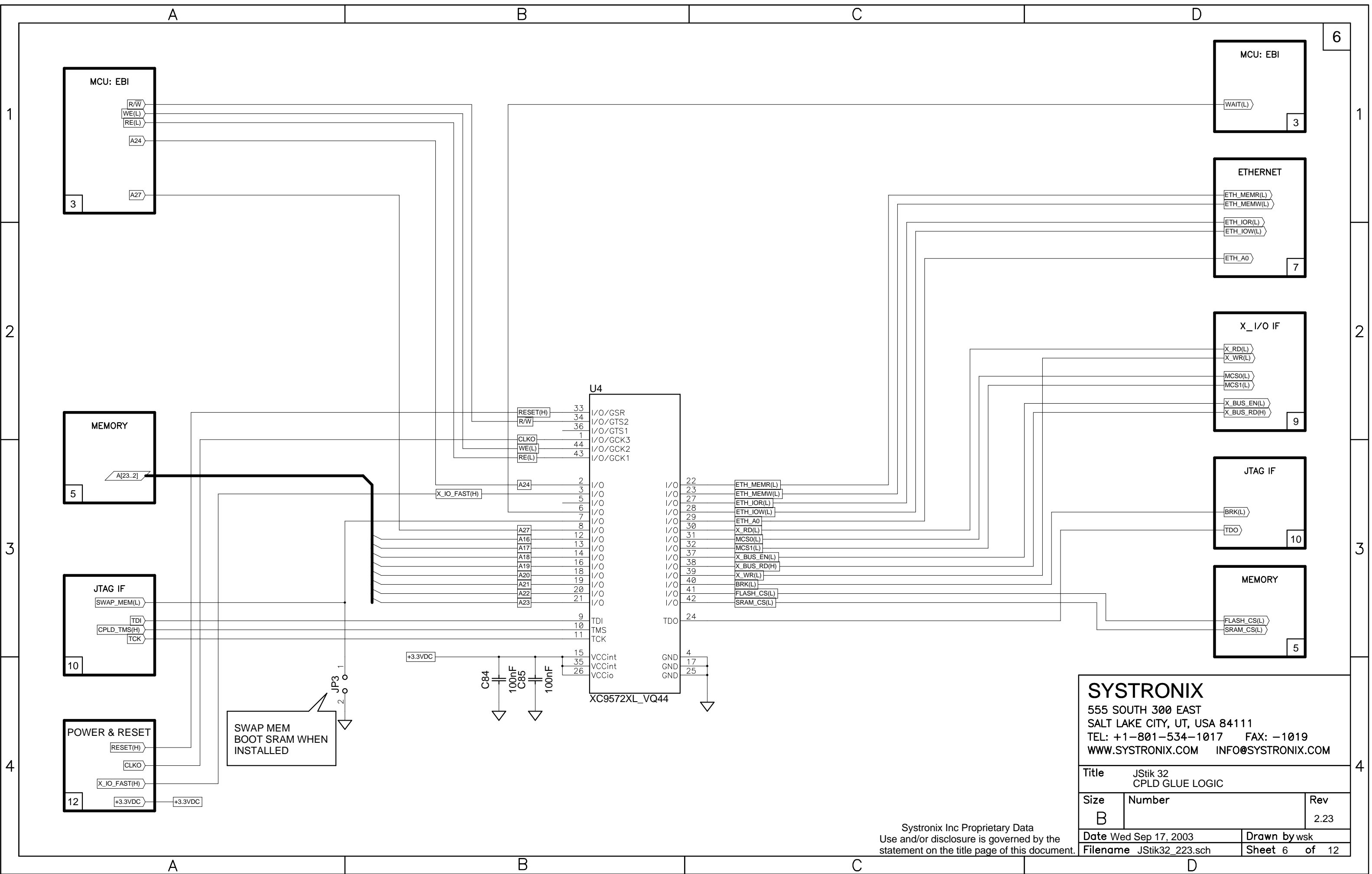
**MEMORY OPTIONS**

FLASH (U16, U18)		SRAM (U9, U12)		
DEVICE	SIZE	DEVICE	SIZE	SPEED
29LV160	4M Bytes	K6F8016	2M Bytes	55nS
29LV320	8M Bytes			

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Title		JStik 32 MEMORY	
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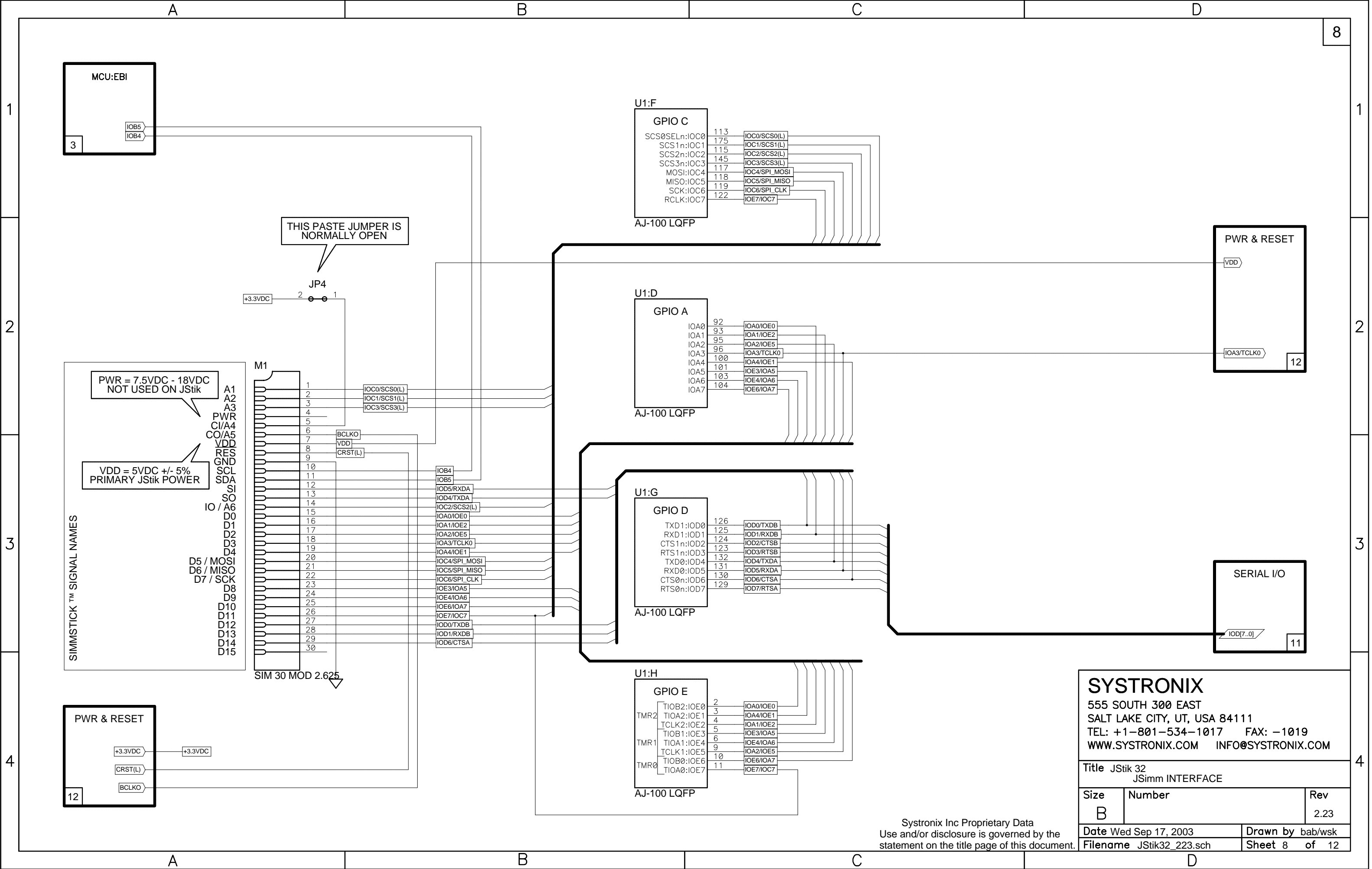


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Title		JStik 32 CPLD GLUE LOGIC	
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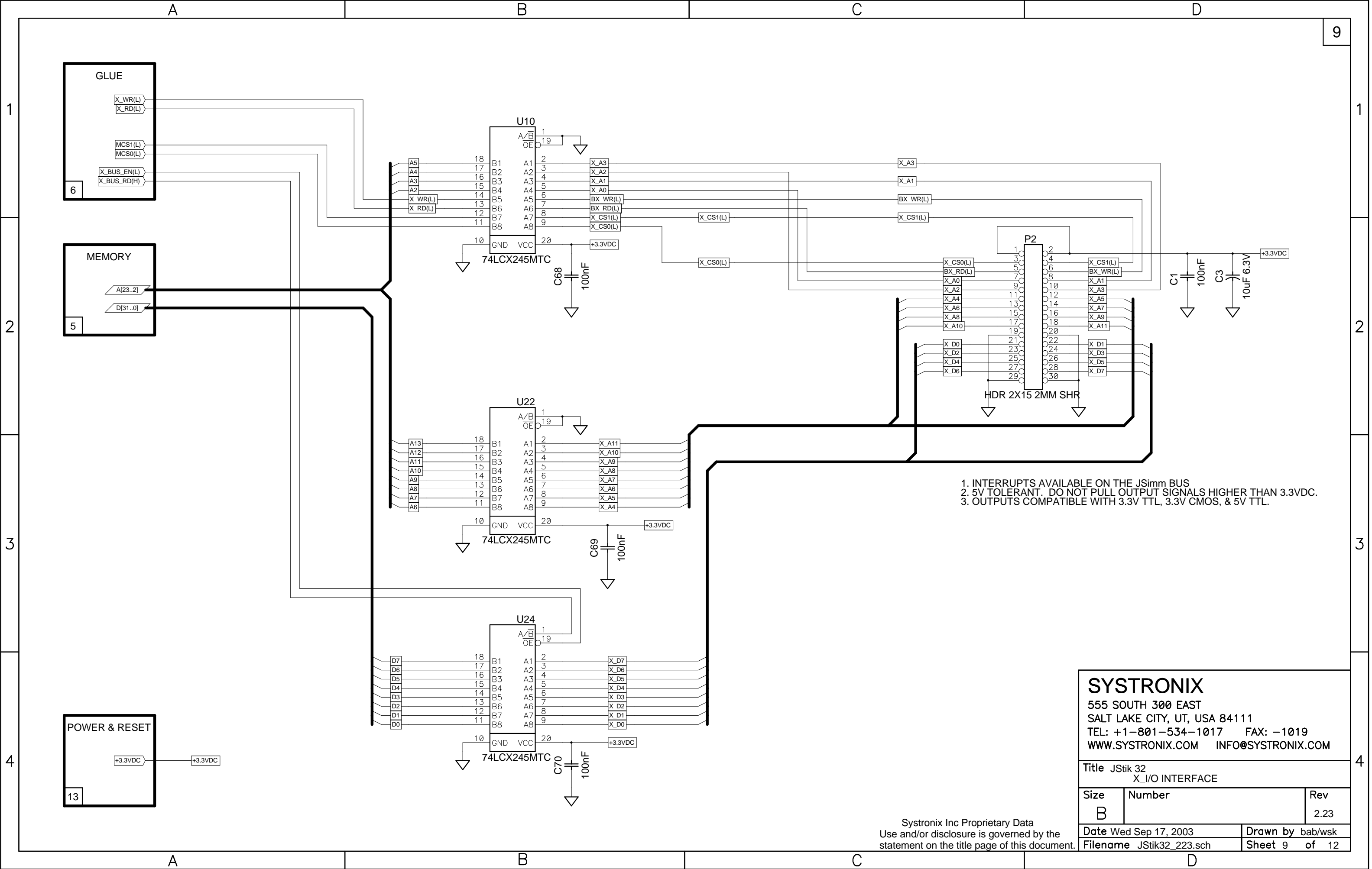




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Filename JSStik32_223.sch	Sheet 8 of 12	

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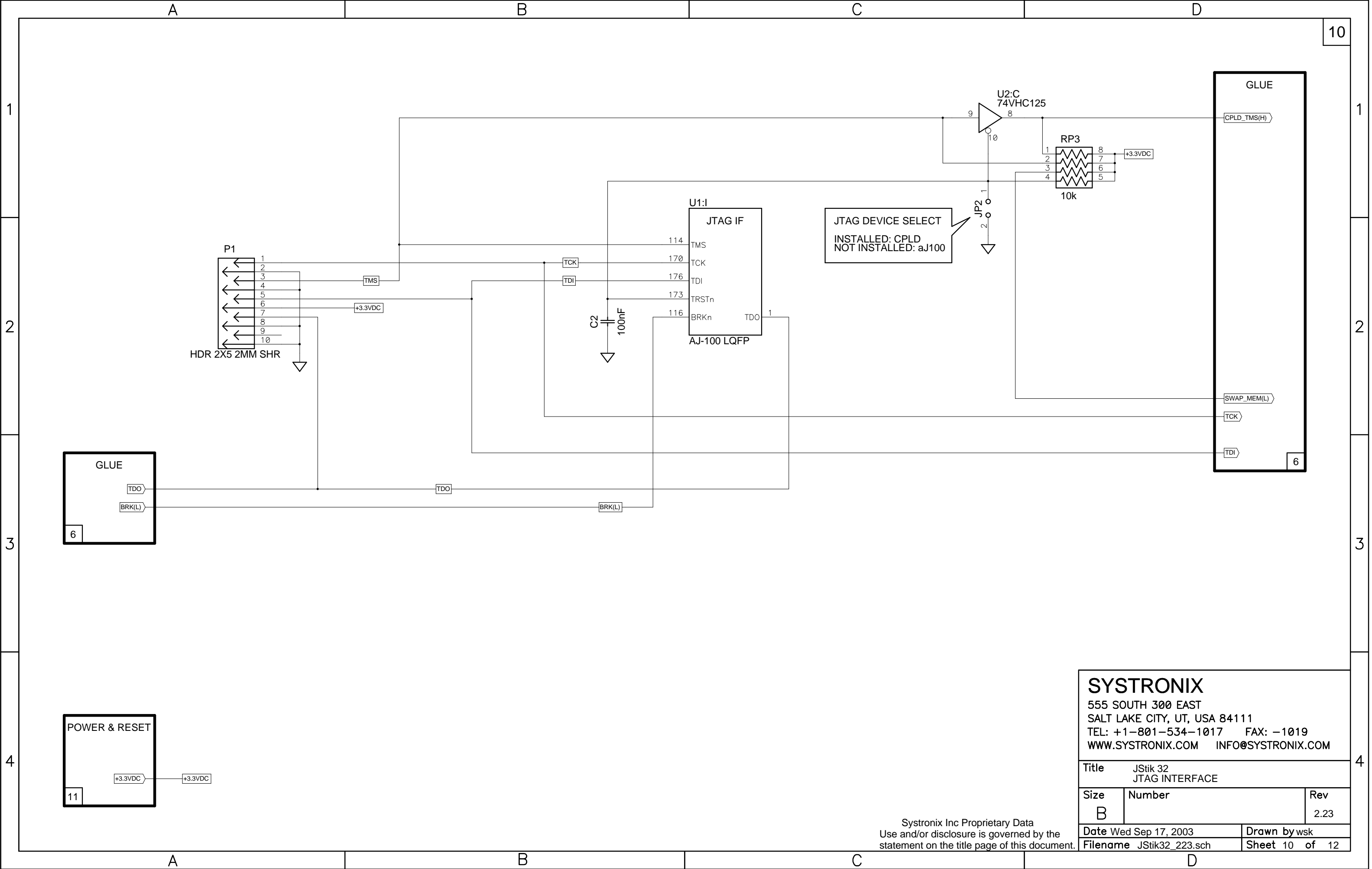


1. INTERRUPTS AVAILABLE ON THE JSimm BUS
2. 5V TOLERANT. DO NOT PULL OUTPUT SIGNALS HIGHER THAN 3.3VDC.
3. OUTPUTS COMPATIBLE WITH 3.3V TTL, 3.3V CMOS, & 5V TTL.

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Title JSStik 32 X_I/O INTERFACE		
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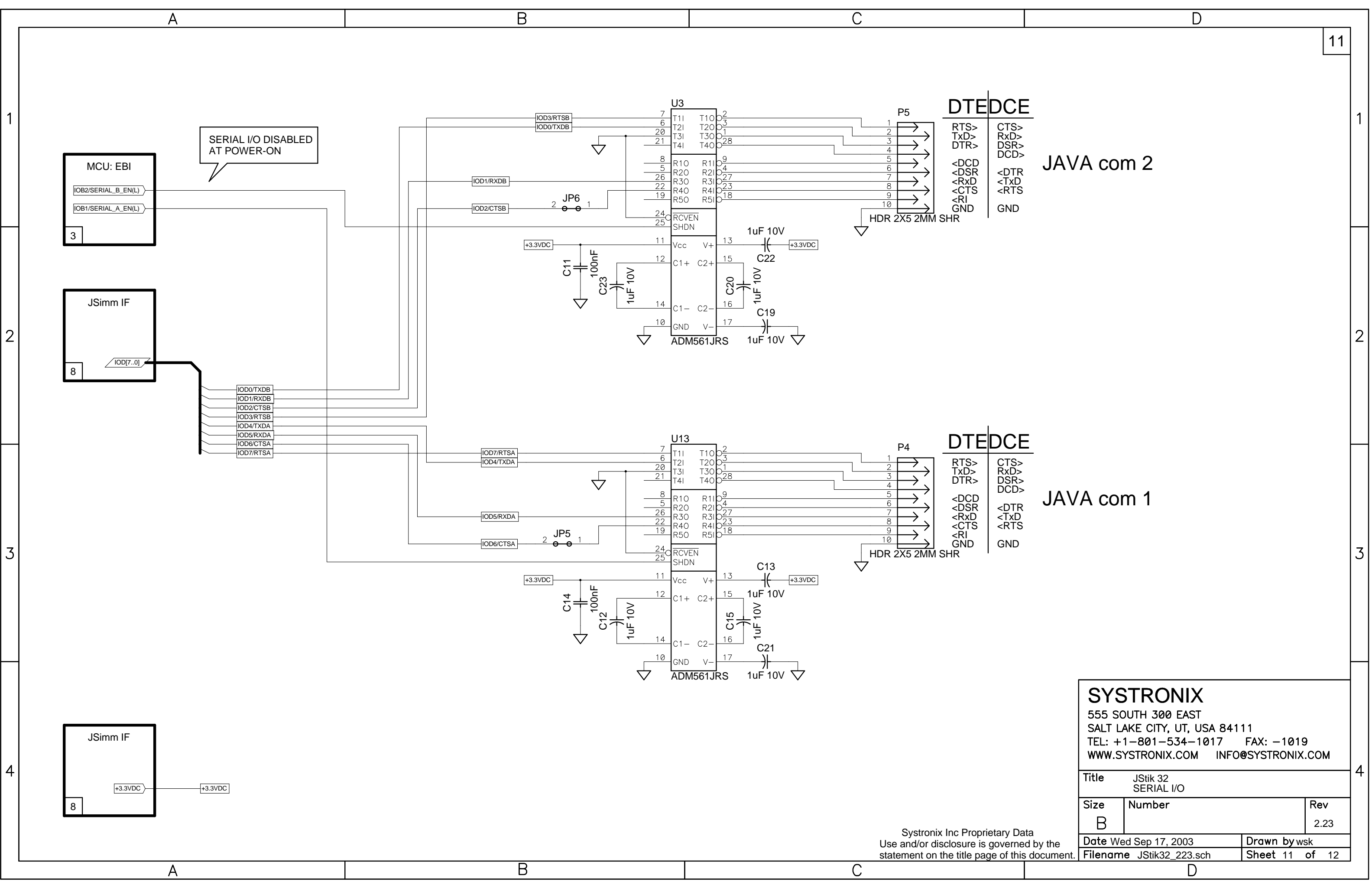


JTAG DEVICE SELECT  
 INSTALLED: CPLD  
 NOT INSTALLED: aJ100

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SERIAL I/O DISABLED AT POWER-ON

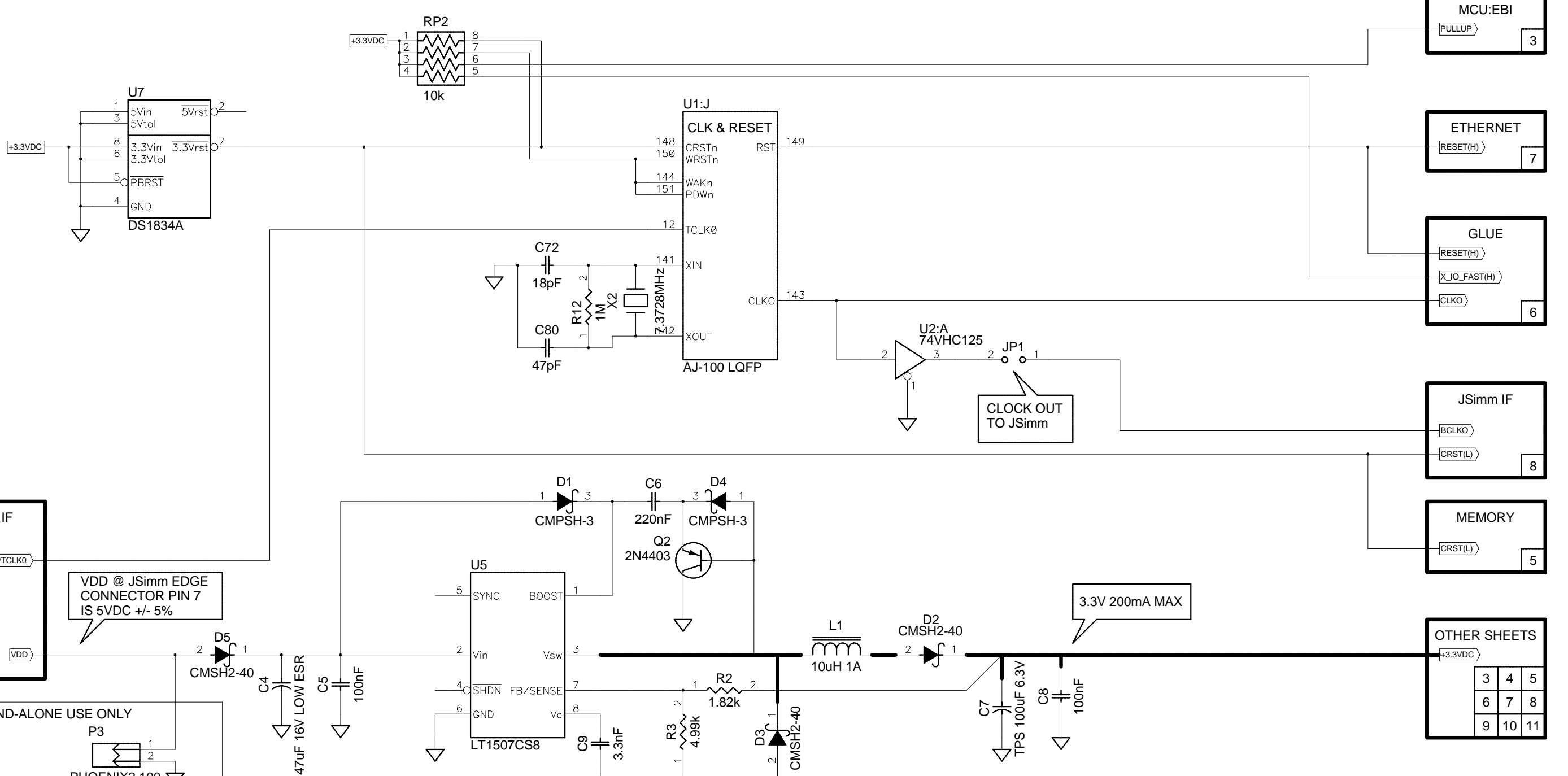
JAVA com 2

JAVA com 1

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Title		JStik 32 SERIAL I/O	
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VDD @ JSim EDGE CONNECTOR PIN 7 IS 5VDC +/- 5%

3.3V 200mA MAX

FOR STAND-ALONE USE ONLY

PHOENIX2 100

5 TO 14 VDC INPUT ONLY WHEN JSim IS USED STAND-ALONE.

VDD (JSim EDGE PIN 7) MUST NOT BE DRIVEN ABOVE 5V WHEN JSim IS INSTALLED IN A SYSTRONIX SOCKET.

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Title	JSim 32 POWER, CLOCK, & RESET	
Size	Number	Rev
B		2.23
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OTHER SHEETS

+3.3VDC		
3	4	5
6	7	8
9	10	11