TStik.72.NB – REVISIONS

SCH REV	PCB REV	DATE	BY	DESCRIPTION
0.0		02 NOV 20	wsk	START (From TStik.72 Rev 0.30)
1.0	1.0	02 DEC 24	wsk	PROTOTYPE LAYOUT COMPLETE
1.10	1.10	03 APR 17	wsk	Sheet 2: Corrected TABLE 3; Sheet 3: Changed U23 supply voltage; Sheet 4: Added RP4C and JP2; Sheet 5: Added RP5; Sheet 6: Changed LED2, LED4, LED6 to green; Changed LED3, LED5, LED7 to yellow; Sheet 7: Changed RX4/TX4 connections to M1; Sheet 8: Changed U9 & U10 supply voltage; Sheet 10: Added Q5; restructured the RESET circuitry;
1.20	1.20	03 JUL 08	wsk	Sheet 6: Disconnected U8 pin 4 from RSTOUT(L) and connected U8 pin 4 to +3.3VDC; Sheet 10: Removed RSTOUT(L) connection to Sheet 6;
1.21	1.20	04 MAR 10	wsk	Sheet 2: Clarifications to TABLE 2 and TABLE 3;
1.30	1.30	04 MAR 15	wsk	Sheet 3: Renamed nets: MISO to CFG_MISO, net at U1 pin 54 (P6.2) to MISO; Sheet 4: Renamed net: MISO to CFG_MISO;
1.31	1.30	04 MAR 24	wsk	Sheet 2: Corrected Timing Diagram annotation;
2.00	2.00	04 AUG 25	wsk	Sheet 2: Modified Tables 2 & 3; Sheet 3: Changed X1 to 15MHz; Sheet 4: Added signal EN2480 and XRX1; Deleted nets CE0(L), CE1(L), SRAM_CE0(L), SRAM_CE1(L), RX0, SIN0; Sheet 5: Added Q6,Q7 and +5VDC; Sheet 7: Added RP5C,RP5D, EN2480, P1.3/TX1, XRX1, SDA, SCL; Sheet 10: Added JP3;
2.01	2.00	04 DEC 08	wsk	Sheet 2: Modified Table 3;
2.10	2.10	05 JAN 17	wsk	Sheet 5: Connected Q6/Q7 gates to RST_CS(L); Sheet 10: Added RST_CS(L); PCB: Connected Simm72 pins 68-69 together on top layer;
2.20	2.10	06 JAN 27	wsk	Sheet 10: Changed U15 to MIC5247-YM5;
2.30	2.20	06 JUN 08	wsk	Sheet 5: Changed U5 to S29AL032D;

PCB REV	DATE	BY

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TO DO:

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Title	Tstik.72.NB REVISIONS	
Size: B	Number	Rev: 2.00
Date: Mon Sep 25, 2006		Drawn by: wsk
Filename: Tstik_72_NB_230.sch		Sheet 1 of 10

TABLE 1 - TStik.MHH FUNCTIONS
1 - SYSTEM RESET LOGIC 2 - SRAM NON-VOLITIZER 3 - SERIAL 1 I/O PATH SELECTION 4 - SERIAL 0 INPUT SOURCE SELECTION * 5 - SIMM72 DATA BUS BUFFER CONTROL * 6 - SYSTEM CONFIGURATION REGISTER (SEE TABLES 2 & 3)

* NOT USED ON TStik.72.NB

TABLE 2 - SYSTEM CONFIGURATION REGISTER (SCR)

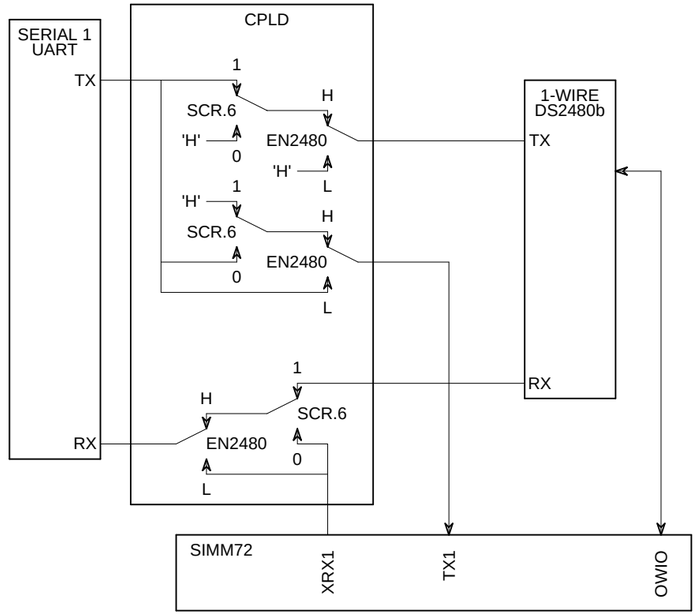
7	6	5	4	3	2	1	0
PERIPH RST	SERIAL 1	CAN/$\overline{\text{I2C}}$	SER 0 TXD EN	ETHERNET DISABLE	NOT USED ON TStik.72.NB		

RESET VALUE == 0x70 SHIFT DIRECTION

TABLE 3 - SYSTEM CONFIGURATION REGISTER BIT DEFINITIONS

BIT 7:	PERIPHERAL RESET	0	DEFAULT. PERIPHERAL RESET (JSIMM PIN 18) NOT ASSERTED (LOW)
		1	PERIPHERAL RESET (JSIMM PIN 18) ASSERTED (HIGH)
BIT 6:	SERIAL 1 SELECT	0	CONNECTS SERIAL 1 TO SIMM72 PINS 14 & 15
		1	DEFAULT. CONNECTS SERIAL 1 TO 1-WIRE IF EN2480 IS HIGH OR TO PINS 14 & 15 IF EN2480 IS LOW
BIT 5:	CAN ENABLE I2C DISABLE	0	CONNECTS I2C SCK & I2C SDA (P1.0 & P1.1) TO SIMM72 PINS 10 & 11
		1	DEFAULT. CONNECTS CAN TX & CAN RX (P5.0 & P5.1) TO SIMM72 PINS 10 & 11
BIT 4:	SERIAL 0 TXD EN	0	SERIAL 0 RS-232 TRANSMITTER DISABLED
		1	DEFAULT. SERIAL 0 RS-232 TRANSMITTER ENABLED
BIT 3:	ETHERNET DISABLE	0	DEFAULT. ETHERNET TRANSCEIVER ENABLED
		1	ETHERNET TRANSCEIVER DISABLED
BIT 2-0:	NOT USED	VALUES WRITTEN MAY BE READ BUT ARE NOT USED ON TStik.72.NB	

POWER ON DEFAULT STATE SHOWN



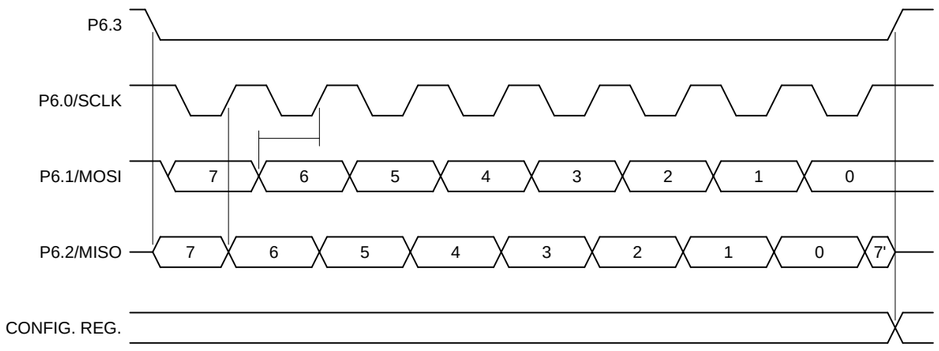


TABLE 4 - ETHERNET MODE SELECTION

JP1-1 2 3	AUTO-NEGOTIATE	SPEED (Mbps)	DUPLEX
	DISABLED*	10*	HALF*
			FULL
		100	HALF
			FULL
	ENABLED	100	HALF
			FULL
		10/100	HALF
			FULL OR HALF

* DEFAULT MODE AS SHIPPED

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Title	Tstik.72.NB NOTES	
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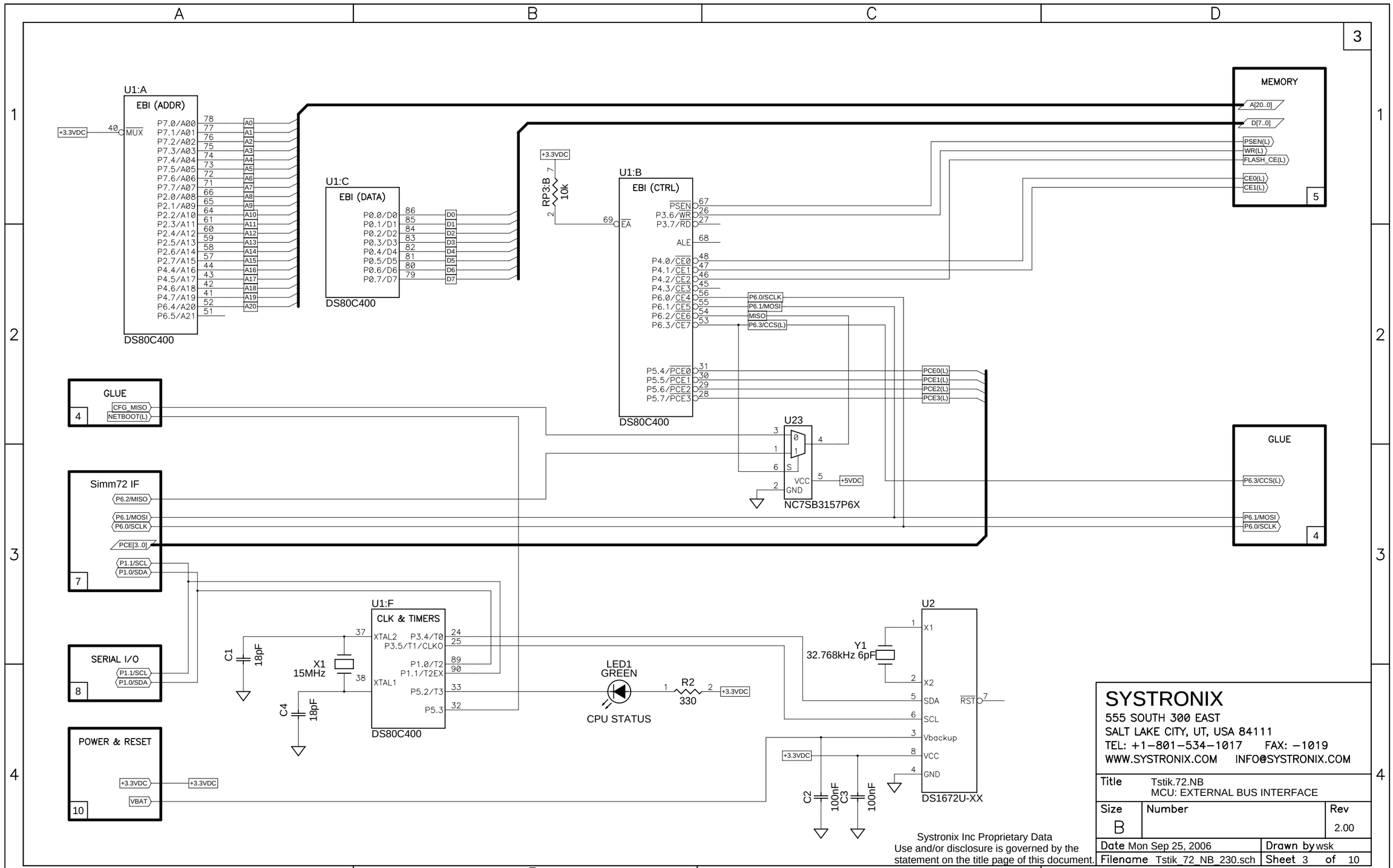

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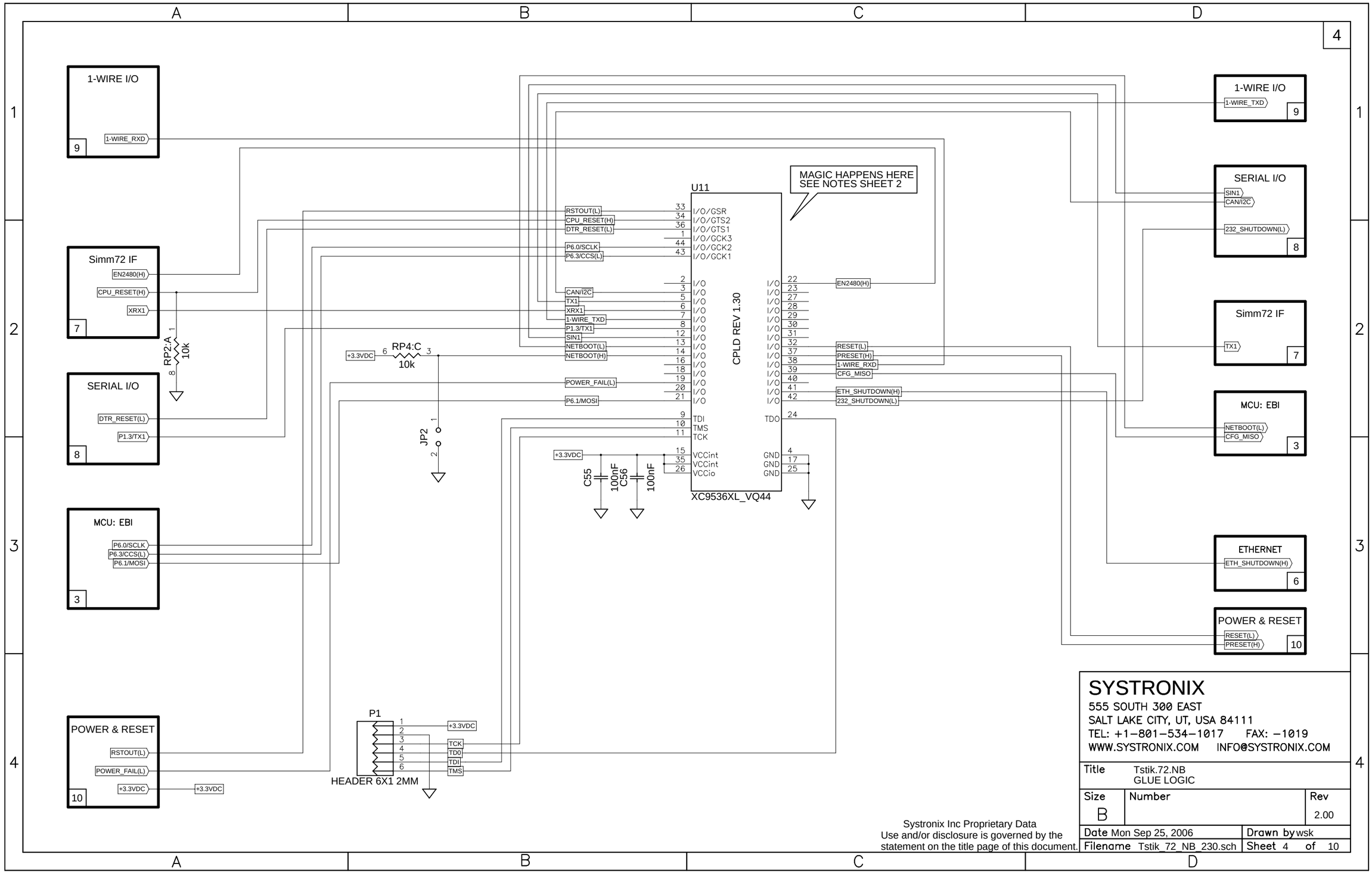

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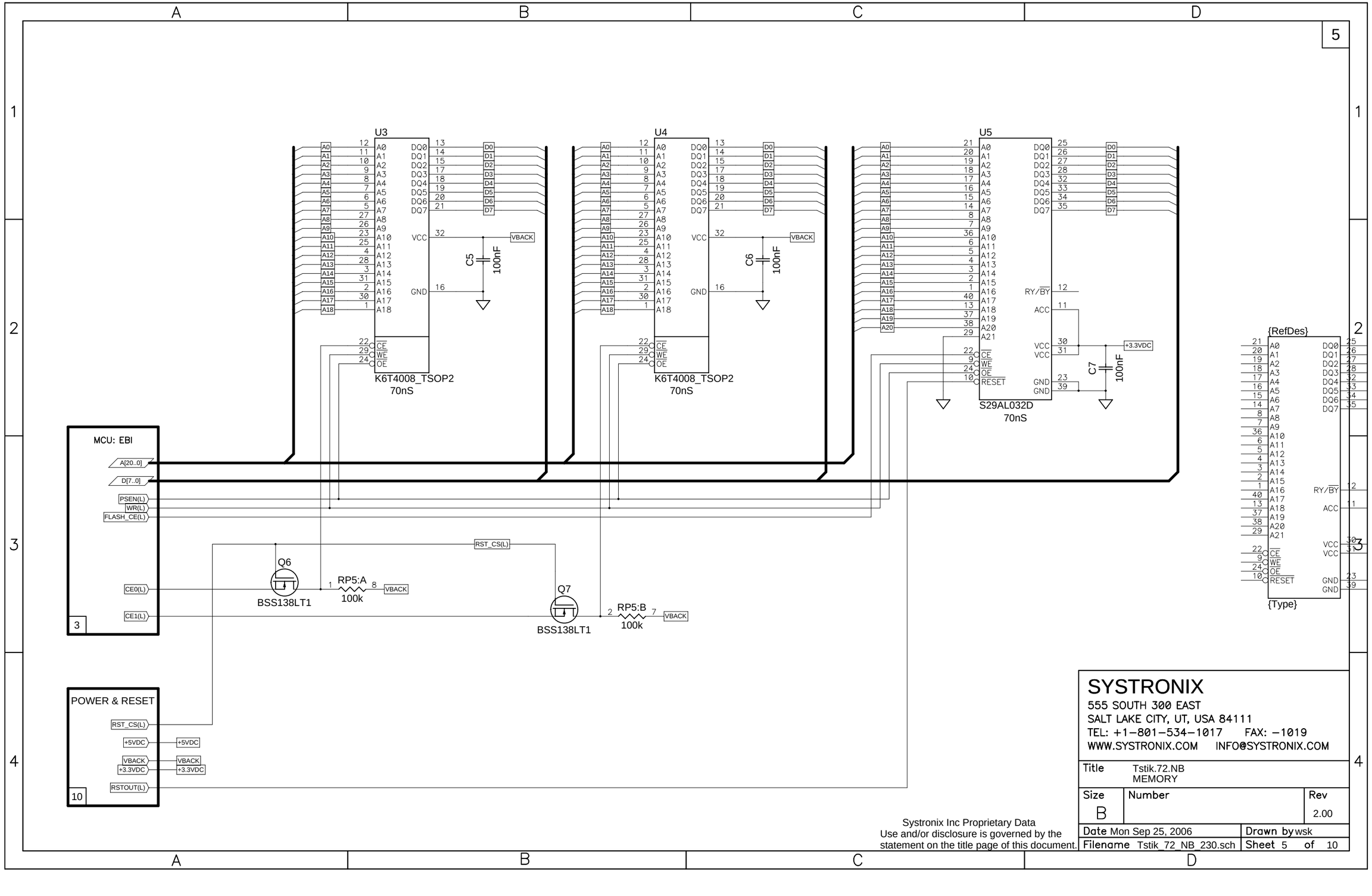

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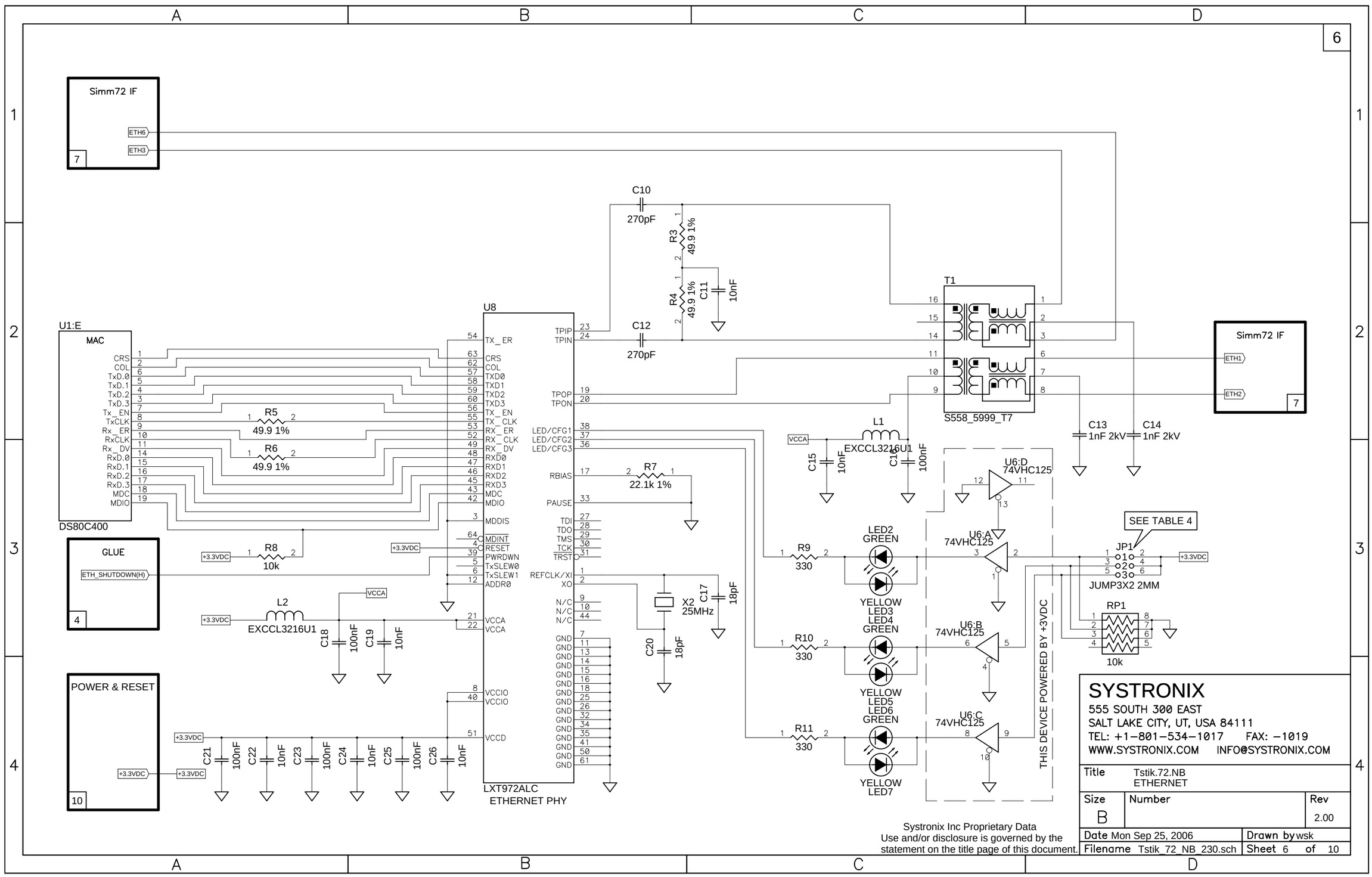

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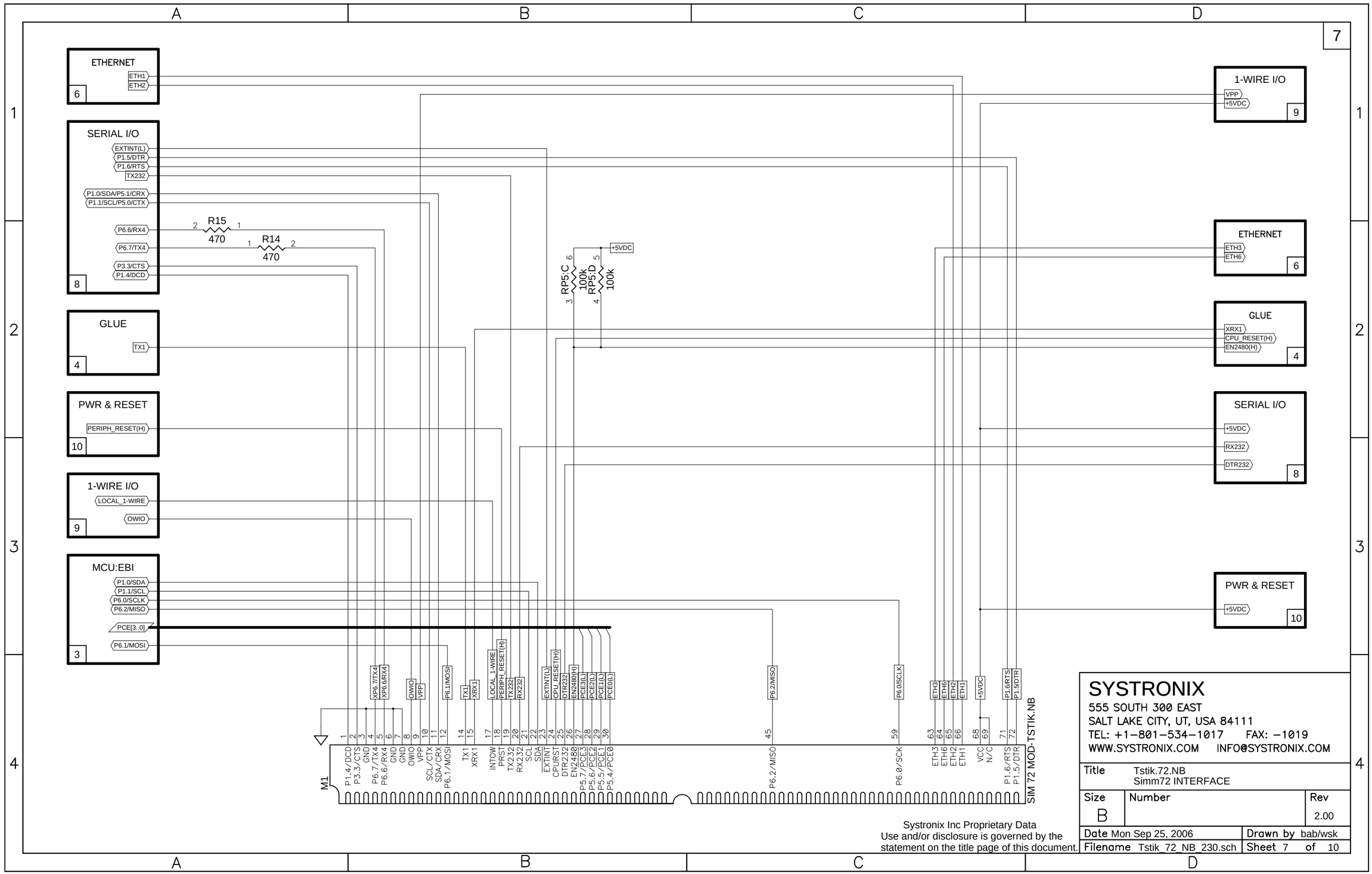
ETHERNET
ETH1
ETH2
6
SERIAL I/O
EXTINT(L)
P1.5/DTR
P1.6/RTS
TX232
P1.0/SDA/P5.1/CRX
P1.1/SCL/P5.0/CTX
P6.6/RX4
P6.7/TX4
P3.3/CTS
P1.4/DCD
8
R15
470
R14
470
GLUE
TX1
4
PWR & RESET
PERIPH_RESET(H)
10
1-WIRE I/O
LOCAL_1-WIRE
OWIO
9
MCU:EBI
P1.0/SDA
P1.1/SCL
P6.0/SCLK
P6.2/MISO
PCE[3..0]
P6.1/MOSI
3
RP5:C
100k
RP5:D
100k
+5VDC
1-WIRE I/O
VPP
+5VDC
9
ETHERNET
ETH3
ETH6
6
GLUE
XRX1
CPU_RESET(H)
EN2480(H)
4
SERIAL I/O
+5VDC
RX232
DTR232
8
PWR & RESET
+5VDC
10
M1
P1.4/DCD
P3.3/CTS
GND
P6.7/TX4
P6.6/RX4
GND
GND
OWIO
VPP
SCL/CTX
SDA/CRX
P6.1/MOSI
TX1
XRX1
INTOW
PRST
TX232
RX232
SCL
SDA
EXTINT
CPURST
DTR232
EN2480
P5.7/PCE3
P5.6/PCE2
P5.5/PCE1
P5.4/PCE0
P6.2/MISO
P6.0/SCK
ETH3
ETH6
ETH2
ETH1
VCC
N/C
P1.6/RTS
P1.5/DTR
SIM 72 MOD-TSTIK.NB
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Simm72 INTERFACE
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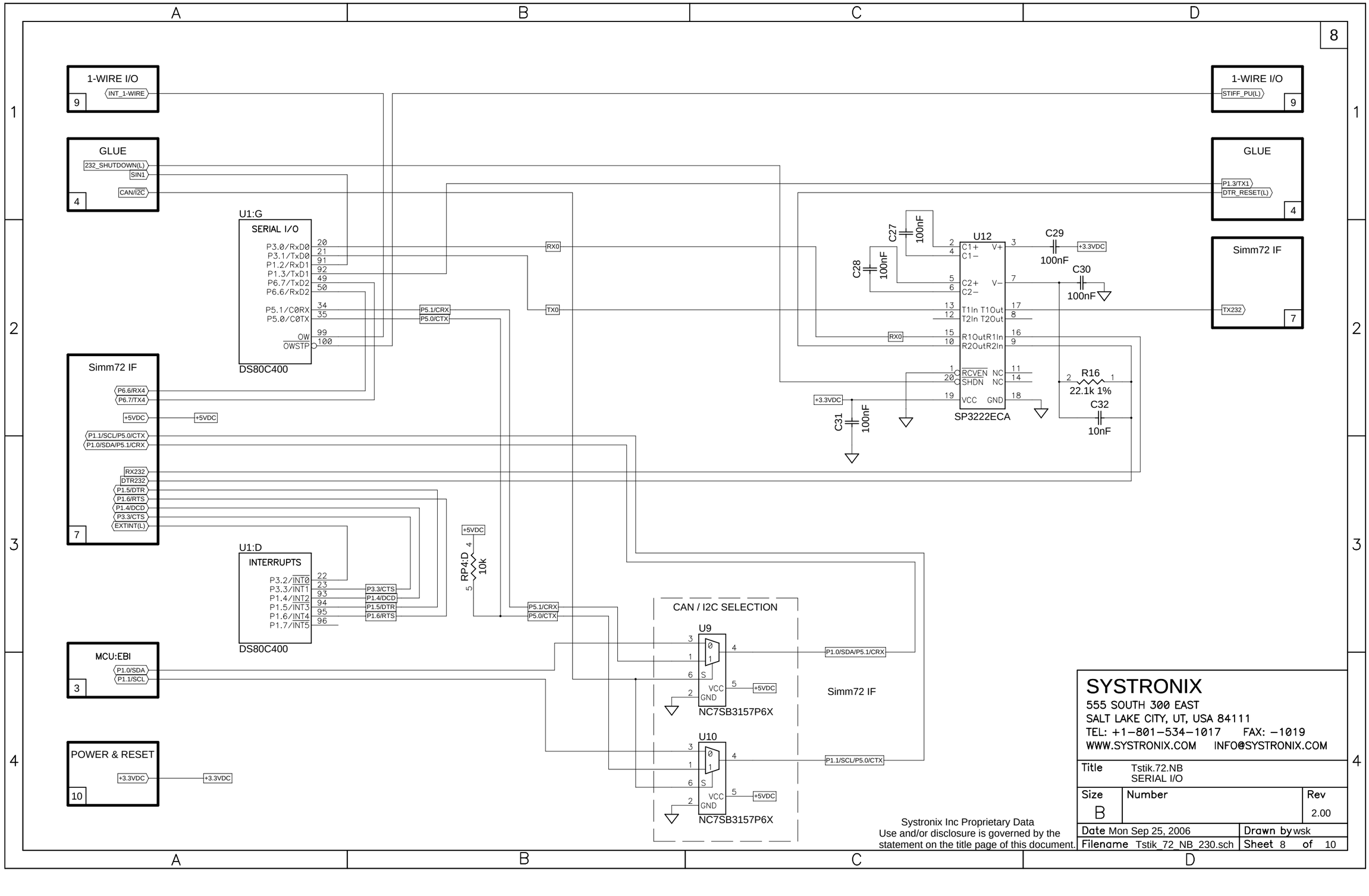
1-WIRE I/O
INT_1-WIRE
9
GLUE
232_SHUTDOWN(L)
SIN1
CAN/I2C
4
U1:G
SERIAL I/O
P3.0/RxD0 20
P3.1/TxD0 21
P1.2/RxD1 91
P1.3/TxD1 92
P6.7/TxD2 49
P6.6/RxD2 50
P5.1/C0RX 34
P5.0/C0TX 35
OW 99
OWSTP 100
DS80C400
RX0
TX0
P5.1/CRX
P5.0/CTX
Simm72 IF
P6.6/RX4
P6.7/TX4
+5VDC
+5VDC
P1.1/SCL/P5.0/CTX
P1.0/SDA/P5.1/CRX
RX232
DTR232
P1.5/DTR
P1.6/RTS
P1.4/DCD
P3.3/CTS
EXTINT(L)
7
U1:D
INTERRUPTS
P3.2/INT0 22
P3.3/INT1 23
P1.4/INT2 93
P1.5/INT3 94
P1.6/INT4 95
P1.7/INT5 96
DS80C400
P3.3/CTS
P1.4/DCD
P1.5/DTR
P1.6/RTS
+5VDC
RP4:D
10k
MCU:EBI
P1.0/SDA
P1.1/SCL
3
POWER & RESET
+3.3VDC
+3.3VDC
10
U12
C1+ 2
C1− 4
C2+ 5
C2− 6
V+ 3
V− 7
T1In 13
T2In 12
T1Out 17
T2Out 8
R1OutR1In 15 16
R2OutR2In 10 9
RCVEN 1
SHDN 20
NC 11
NC 14
VCC 19
GND 18
SP3222ECA
C27 100nF
C28 100nF
C29 100nF
C30 100nF
C31 100nF
C32 10nF
R16 22.1k 1%
+3.3VDC
RX0
TX0
1-WIRE I/O
STIFF_PU(L)
9
GLUE
P1.3/TX1
DTR_RESET(L)
4
Simm72 IF
TX232
7
CAN / I2C SELECTION
U9
U10
NC7SB3157P6X
NC7SB3157P6X
P1.0/SDA/P5.1/CRX
P1.1/SCL/P5.0/CTX
Simm72 IF
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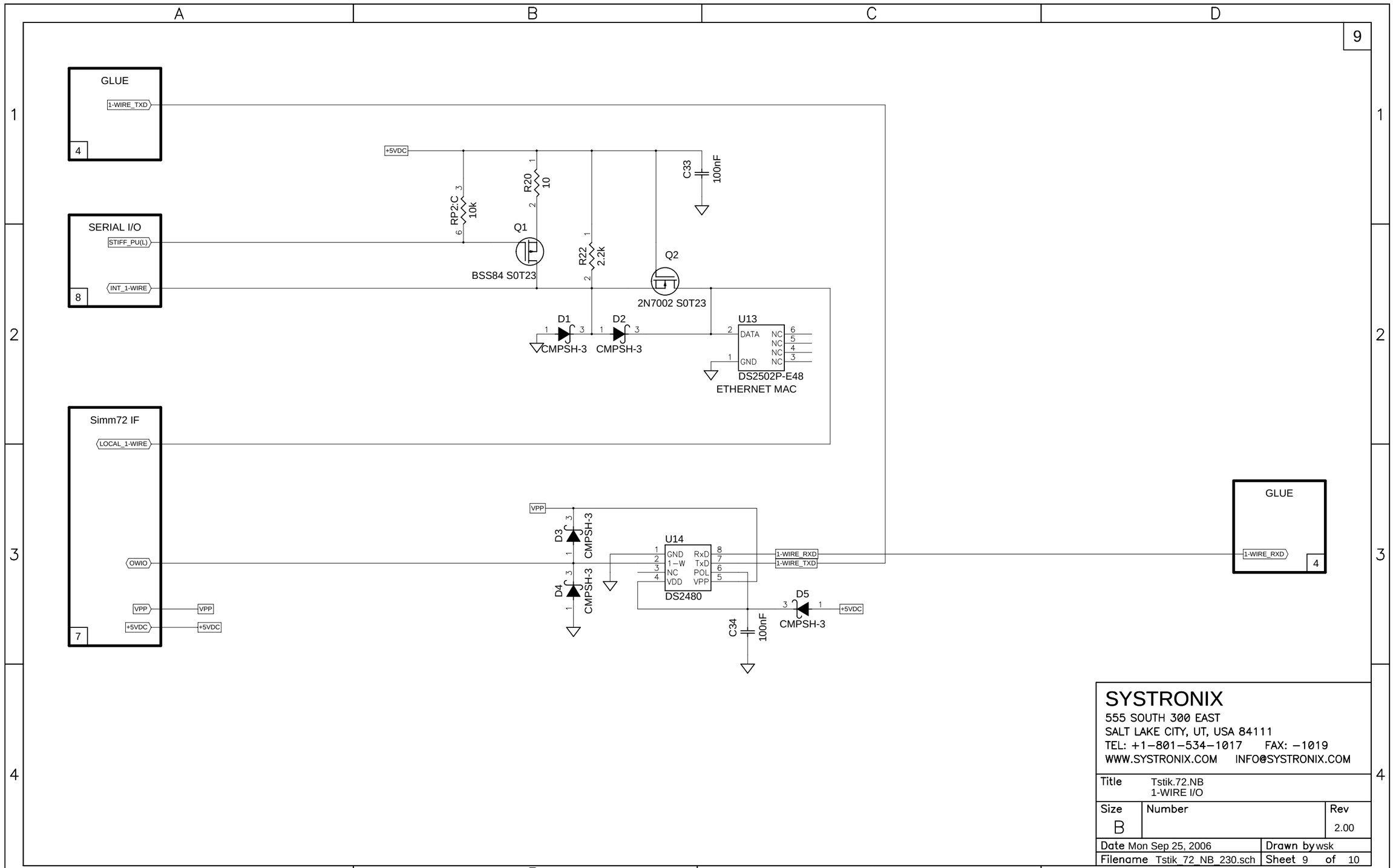

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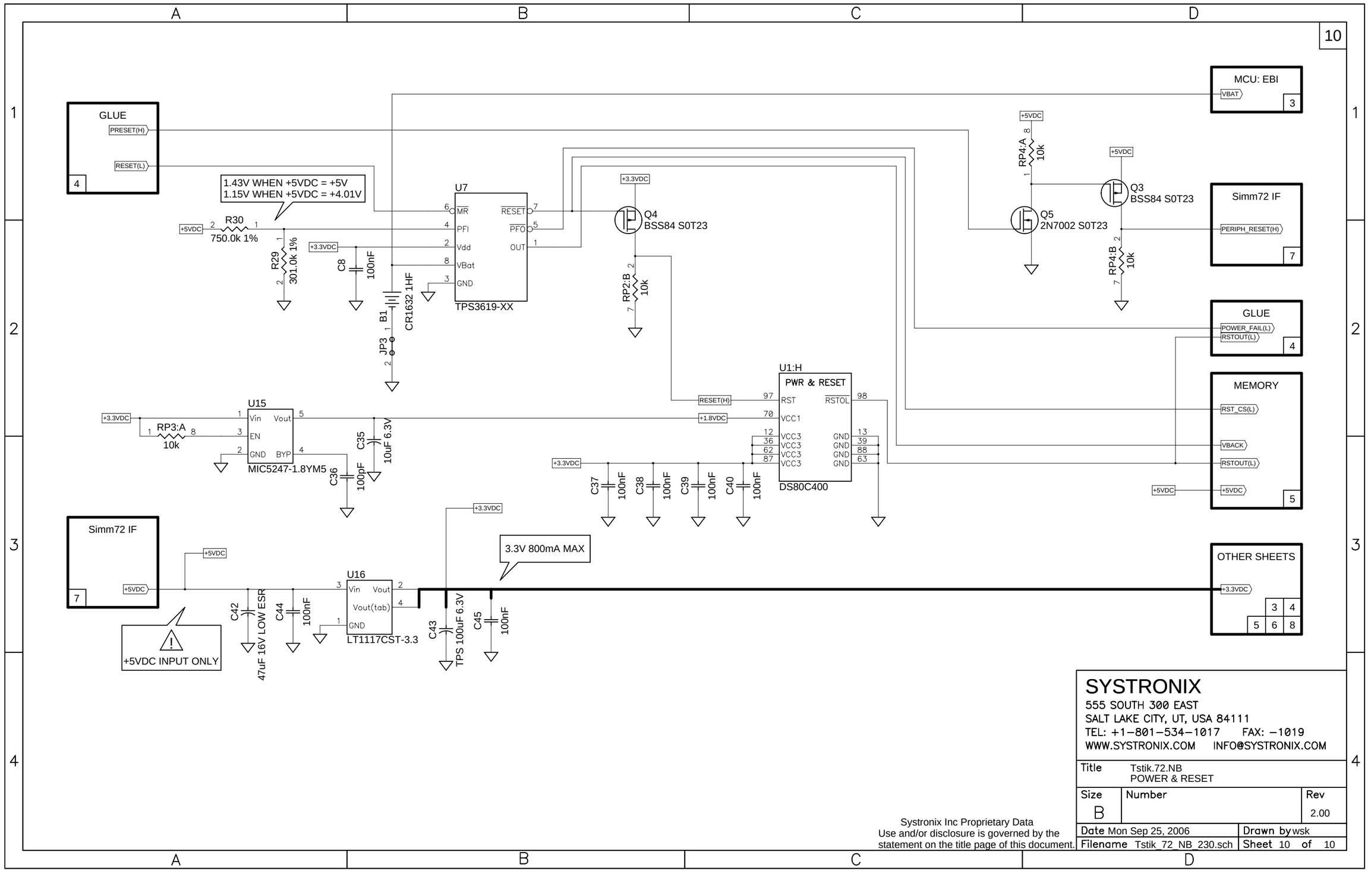
GLUE
PRESET(H)
RESET(L)
4
1.43V WHEN +5VDC = +5V
1.15V WHEN +5VDC = +4.01V
+5VDC
R30
750.0k 1%
R29
301.0k 1%
+3.3VDC
C8
100nF
JP3
B1
CR1632 1HF
U7
MR
PFI
Vdd
VBat
GND
RESET
PFO
OUT
TPS3619-XX
+3.3VDC
Q4
BSS84 S0T23
RP2:B
10k
MCU: EBI
VBAT
3
+5VDC
RP4:A
10k
Q5
2N7002 S0T23
+5VDC
Q3
BSS84 S0T23
RP4:B
10k
Simm72 IF
PERIPH_RESET(H)
7
GLUE
POWER_FAIL(L)
RSTOUT(L)
4
MEMORY
RST_CS(L)
VBACK
RSTOUT(L)
+5VDC
+5VDC
5
U1:H
PWR & RESET
RESET(H)
RST
RSTOL
VCC1
VCC3
VCC3
VCC3
VCC3
GND
GND
GND
GND
DS80C400
+1.8VDC
+3.3VDC
C37
100nF
C38
100nF
C39
100nF
C40
100nF
U15
Vin
Vout
EN
GND
BYP
MIC5247-1.8YM5
+3.3VDC
RP3:A
10k
C35
10uF 6.3V
C36
100pF
Simm72 IF
+5VDC
7
+5VDC INPUT ONLY
U16
Vin
Vout
Vout(tab)
GND
LT1117CST-3.3
C42
47uF 16V LOW ESR
C44
100nF
C43
TPS 100uF 6.3V
C45
100nF
+3.3VDC
3.3V 800mA MAX
OTHER SHEETS
+3.3VDC
3
4
5
6
8
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POWER & RESET
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