

TStik.72.NB – REVISIONS

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SCH REV	PCB REV	DATE	BY	DESCRIPTION	PCB REV	DATE	BY
0.0		02 NOV 20	wsk	START (From TStik.72 Rev 0.30)			
1.0	1.0	02 DEC 24	wsk	PROTOTYPE LAYOUT COMPLETE			
1.10	1.10	03 APR 17	wsk	Sheet 2: Corrected TABLE 3; Sheet 3: Changed U23 supply voltage; Sheet 4: Added RP4C and JP2; Sheet 5: Added RP5; Sheet 6: Changed LED2, LED4, LED6 to green; Changed LED3, LED5, LED7 to yellow; Sheet 7: Changed RX4/TX4 connections to M1; Sheet 8: Changed U9 & U10 supply voltage; Sheet 10: Added Q5; restructured the RESET circuitry;			
1.20	1.20	03 JUL 08	wsk	Sheet 6: Disconnected U8 pin 4 from RSTOUT(L) and connected U8 pin 4 to +3.3VDC; Sheet 10: Removed RSTOUT(L) connection to Sheet 6;			
1.21	1.20	04 MAR 10	wsk	Sheet 2: Clarifications to TABLE 2 and TABLE 3;			
1.30	1.30	04 MAR 15	wsk	Sheet 3: Renamed nets: MISO to CFG_MISO, net at U1 pin 54 (P6.2) to MISO; Sheet 4: Renamed net: MISO to CFG_MISO;			
1.31	1.30	04 MAR 24	wsk	Sheet 2: Corrected Timing Diagram annotation;			
2.00	2.00	04 AUG 25	wsk	Sheet 2: Modified Tables 2 & 3; Sheet 3: Changed X1 to 15MHz; Sheet 4: Added signal EN2480 and XRX1; Deleted nets CE0(L), CE1(L), SRAM_CE0(L), SRAM_CE1(L), RX0, SIN0; Sheet 5: Added Q6,Q7 and +5VDC; Sheet 7: Added RP5C,RP5D, EN2480, P1.3/TX1, XRX1, SDA, SCL; Sheet 10: Added JP3;			
2.01	2.00	04 DEC 08	wsk	Sheet 2: Modified Table 3;			
2.10	2.10	05 JAN 17	wsk	Sheet 5: Connected Q6/Q7 gates to RST_CS(L); Sheet 10: Added RST_CS(L); PCB: Connected Smm72 pins 68-69 together on top layer;			

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TO DO:

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TABLE 1 - TSİK/MHH FUNCTIONS
1 - SYSTEM RESET LOGIC 2 - SRAM NON-VOLATIZER 3 - SERIAL 1 IO PATH SELECTION 4 - SERIAL 0 INPUT SOURCE SELECTION* 5 - SIMM72 DATA BUS BUFFER CONTROL* 6 - SYSTEM CONFIGURATION REGISTER (SEE TABLES 2 & 3)

* NOT USED ON TSİK72NB

TABLE 2 - SYSTEM CONFIGURATION REGISTER (SCR)							
7	6	5	4	3	2	1	0
PERIPH RST	SERIAL 1	CAN/ I2C	SER 0 TXD EN	ETHERNET DISABLE	NOT USED ON TSİK72NB		

RESET VALUE = 0x70

SHIFT DIRECTION

TABLE 3 - SYSTEM CONFIGURATION REGISTER BIT DEFINITIONS			
BIT 7:	PERIPHERAL RESET	0	DEFAULT. PERIPHERAL RESET (JSIMM PIN 18) NOT ASSERTED (LOW)
		1	PERIPHERAL RESET (JSIMM PIN 18) ASSERTED (HIGH)
BIT 6:	SERIAL 1 SELECT	0	CONNECTS SERIAL 1 TO SIMM72 PINS 14 & 15
		1	DEFAULT. CONNECTS SERIAL 1 TO 1-WIRE IF EN2480 IS HIGH OR TO PINS 14 & 15 IF EN2480 IS LOW
BIT 5:	CAN ENABLE I2C DISABLE	0	CONNECTS I2C SCK & I2C SDA (P1.0 & P1.1) TO SIMM72 PINS 10 & 11
		1	DEFAULT. CONNECTS CAN TX & CAN RX (P5.0 & P5.1) TO SIMM72 PINS 10 & 11
BIT 4:	SERIAL 0 TXD EN	0	SERIAL 0 RS-232 TRANSMITTER DISABLED
		1	DEFAULT. SERIAL 0 RS-232 TRANSMITTER ENABLED
BIT 3:	ETHERNET DISABLE	0	DEFAULT. ETHERNET TRANSCEIVER ENABLED
		1	ETHERNET TRANSCEIVER DISABLED
BIT 2:0:	NOT USED	VALUES WRITTEN MAY BE READ BUT ARE NOT USED ON TSİK72NB	

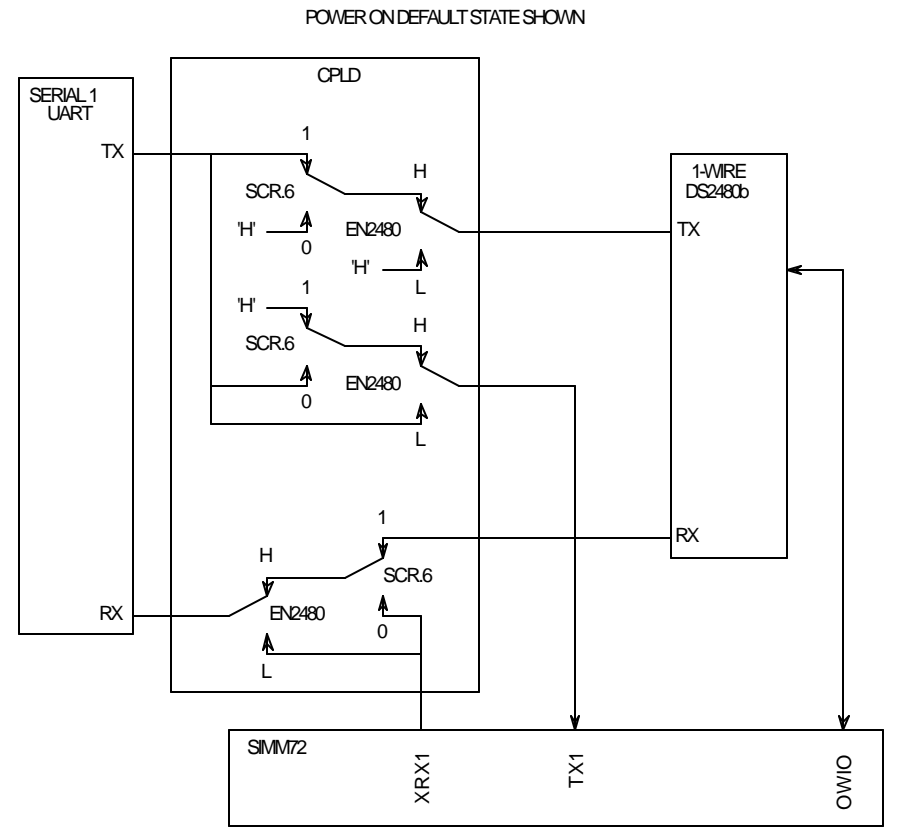
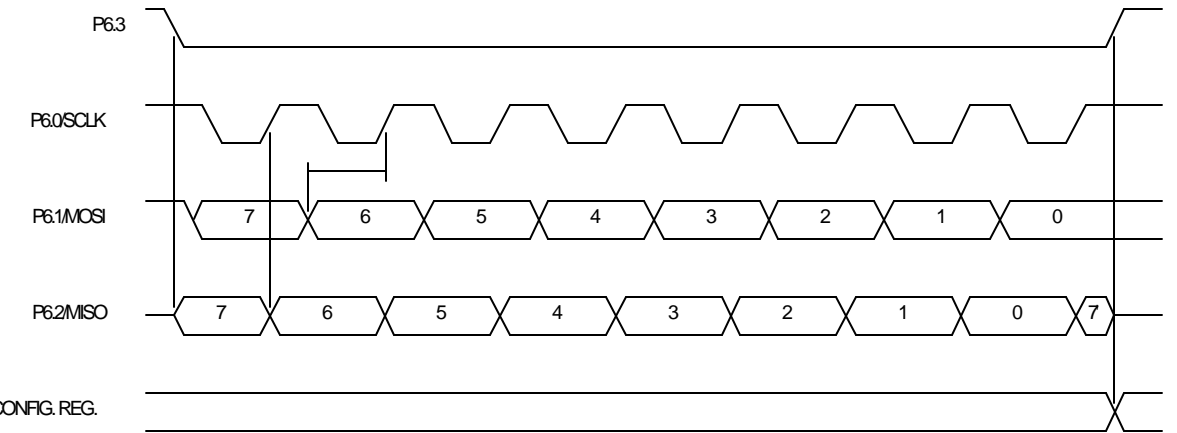


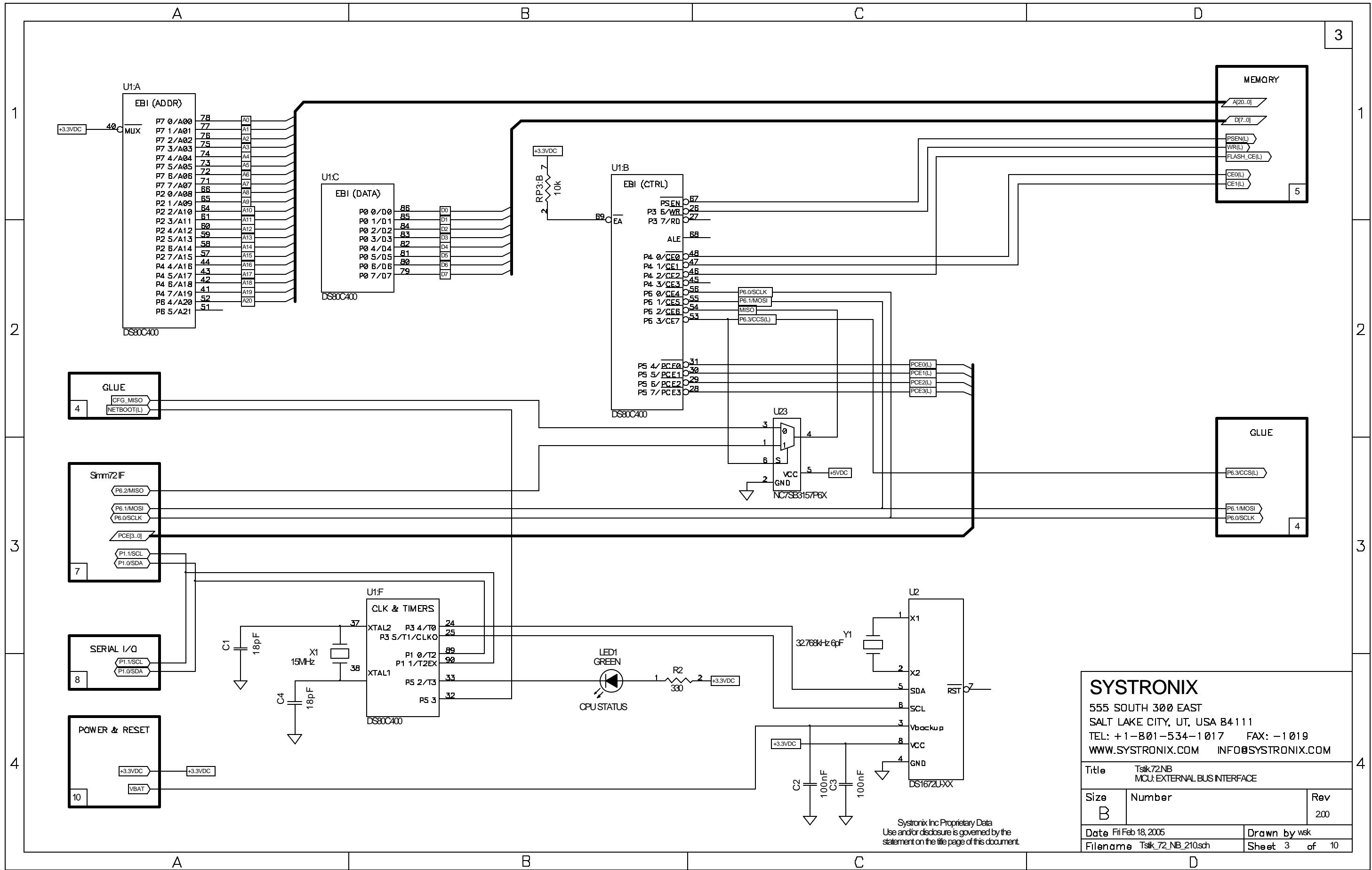
TABLE 4 - ETHERNET MODE SELECTION			
JP1- 1 2 3	AUTO-NEGOTIATE	SPEED (Mbps)	DUPLEX
0 0 0	DISABLED *	10 *	HALF *
0 0 1			FULL
0 1 0		100	HALF
0 1 1		100	FULL
1 0 0	ENABLED	100	HALF
1 0 1			FULL
1 1 1		10/100	FULL OR HALF

* DEFAULT MODE AS SHIPPED

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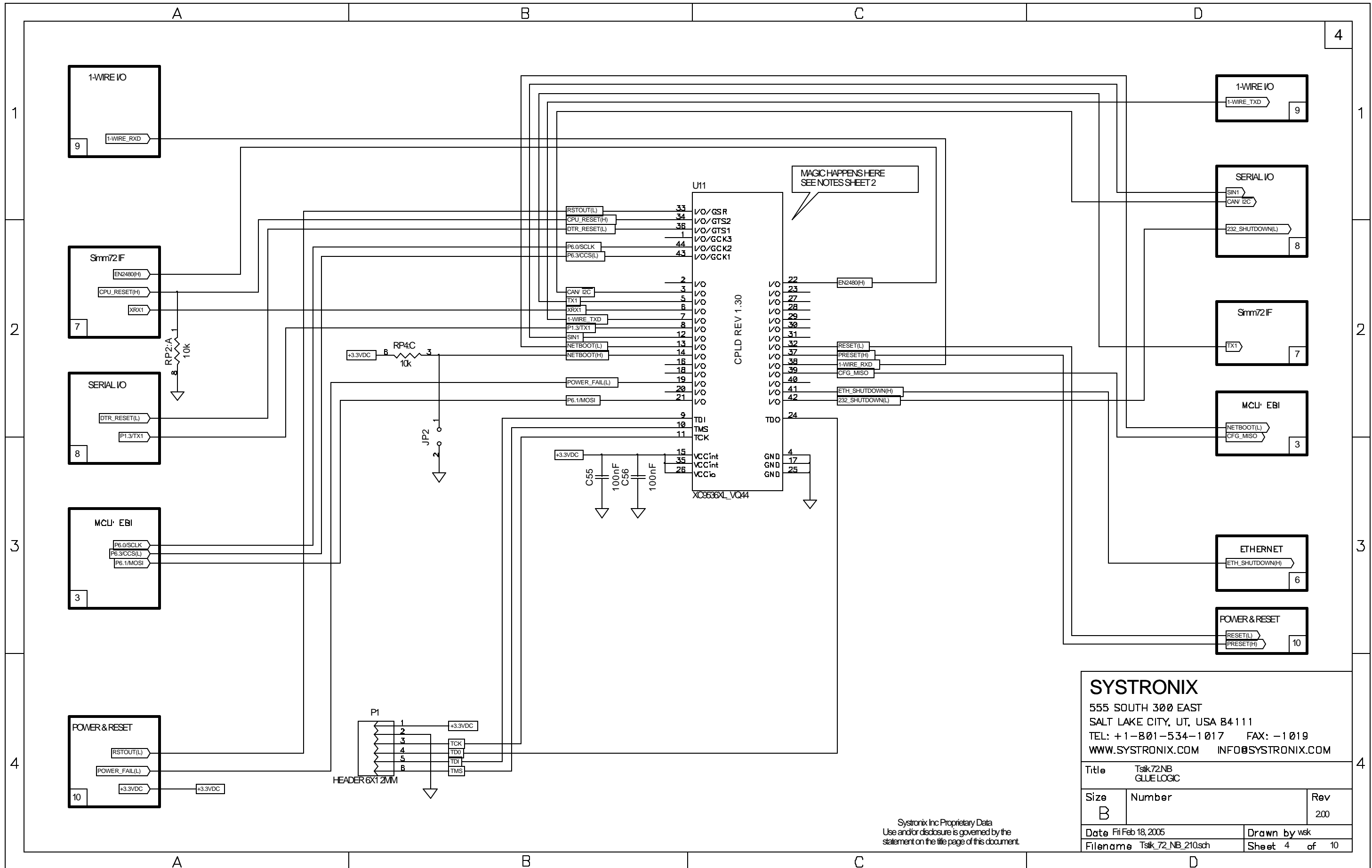
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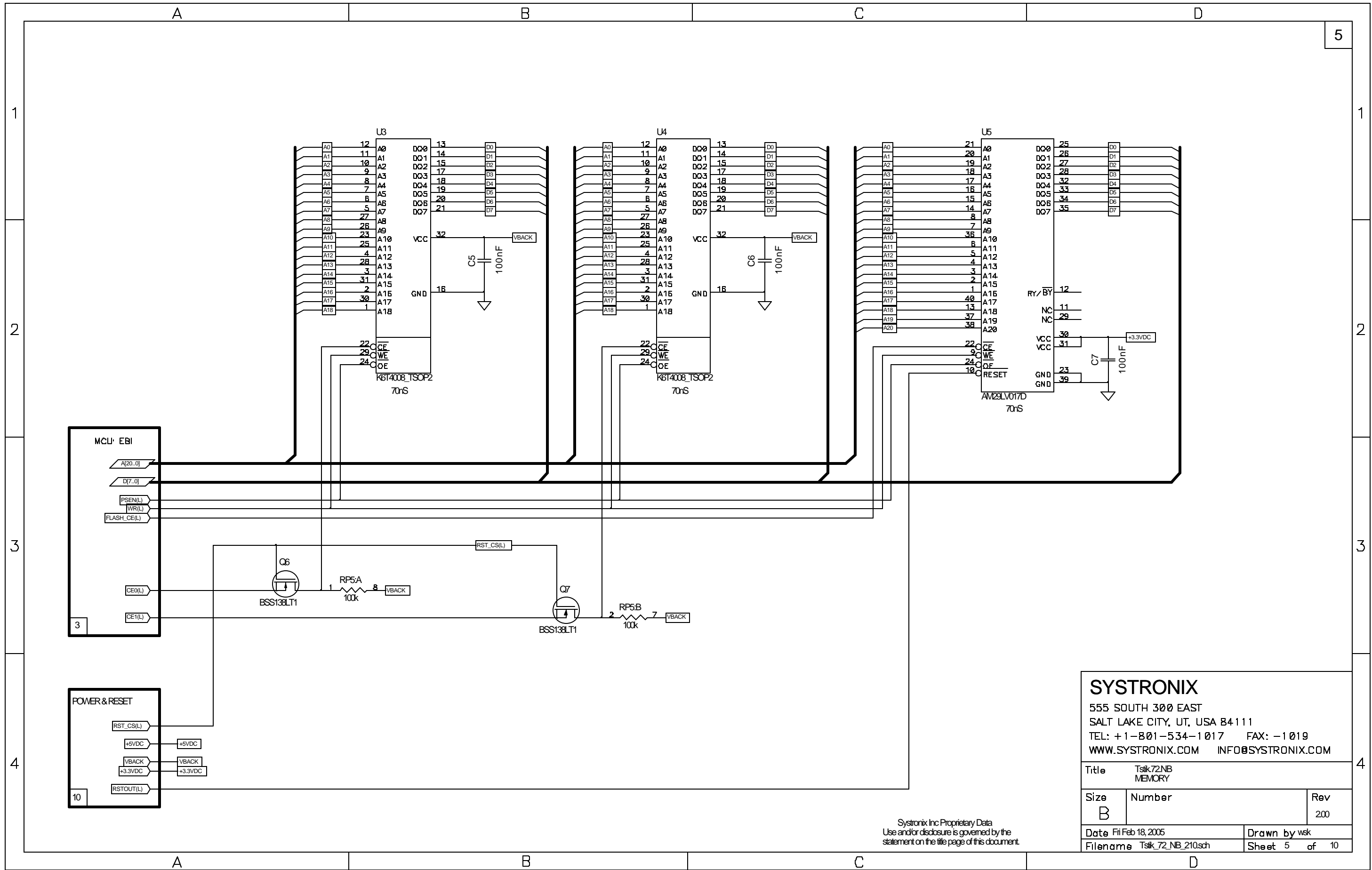
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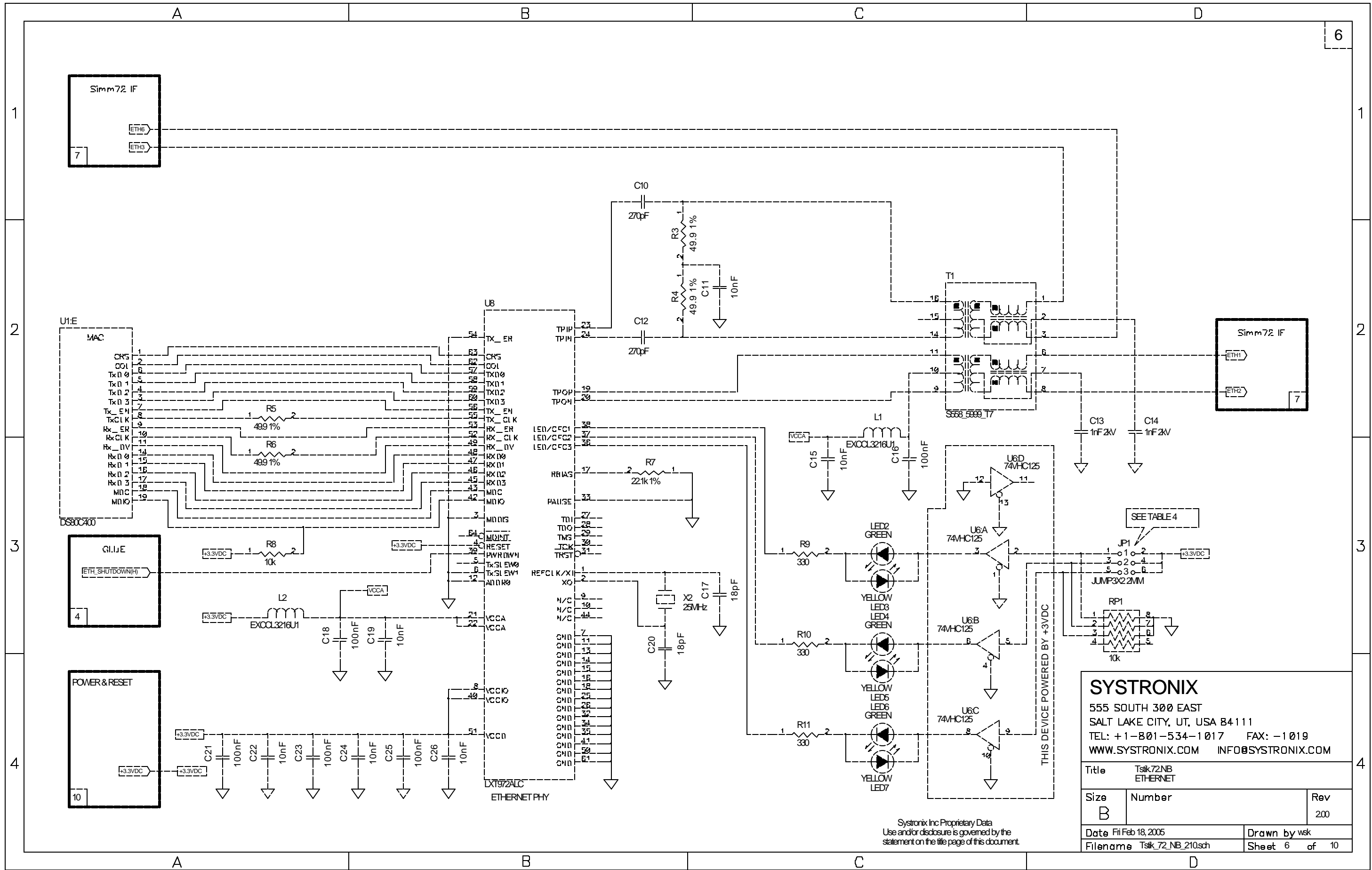
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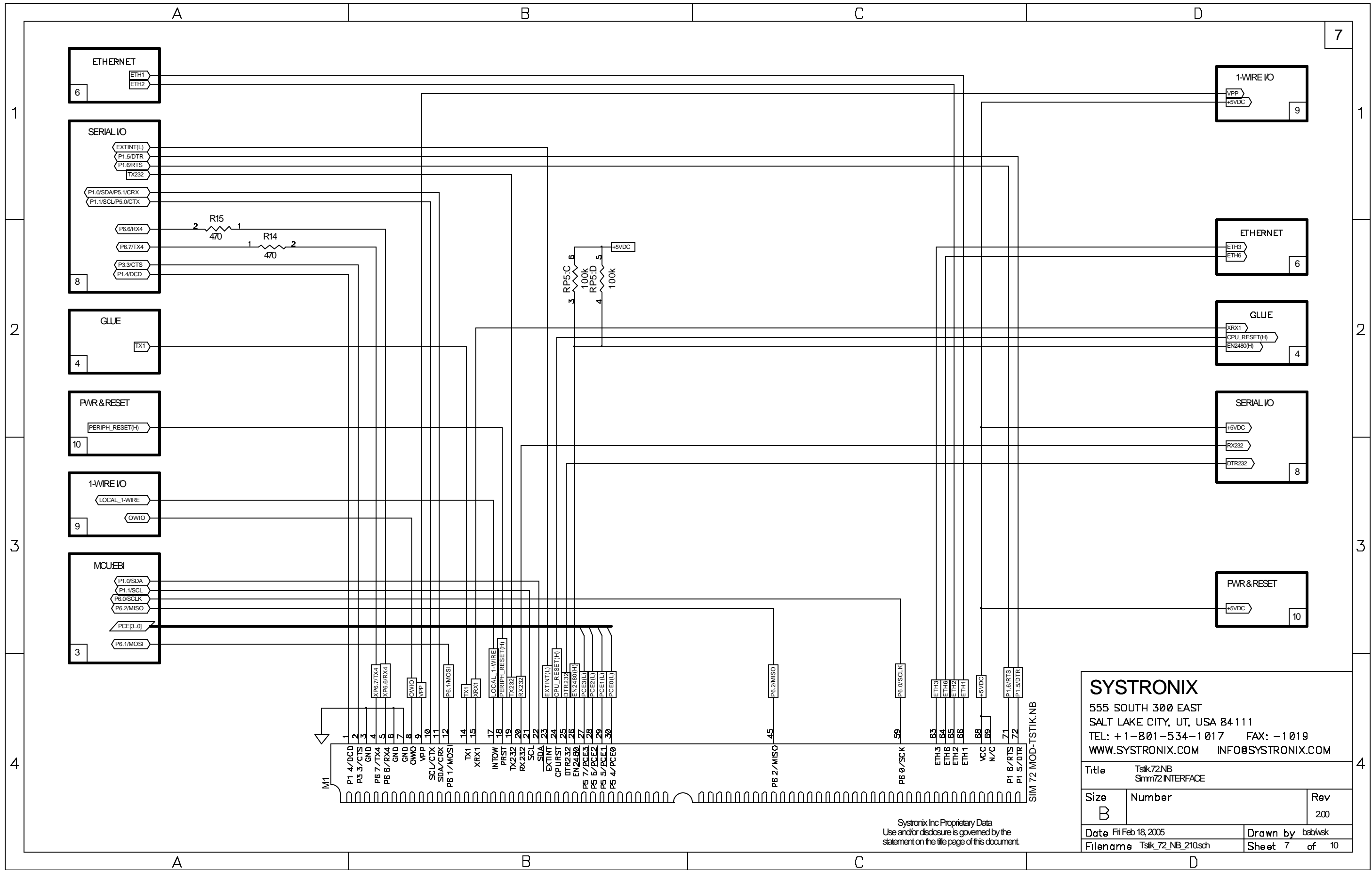
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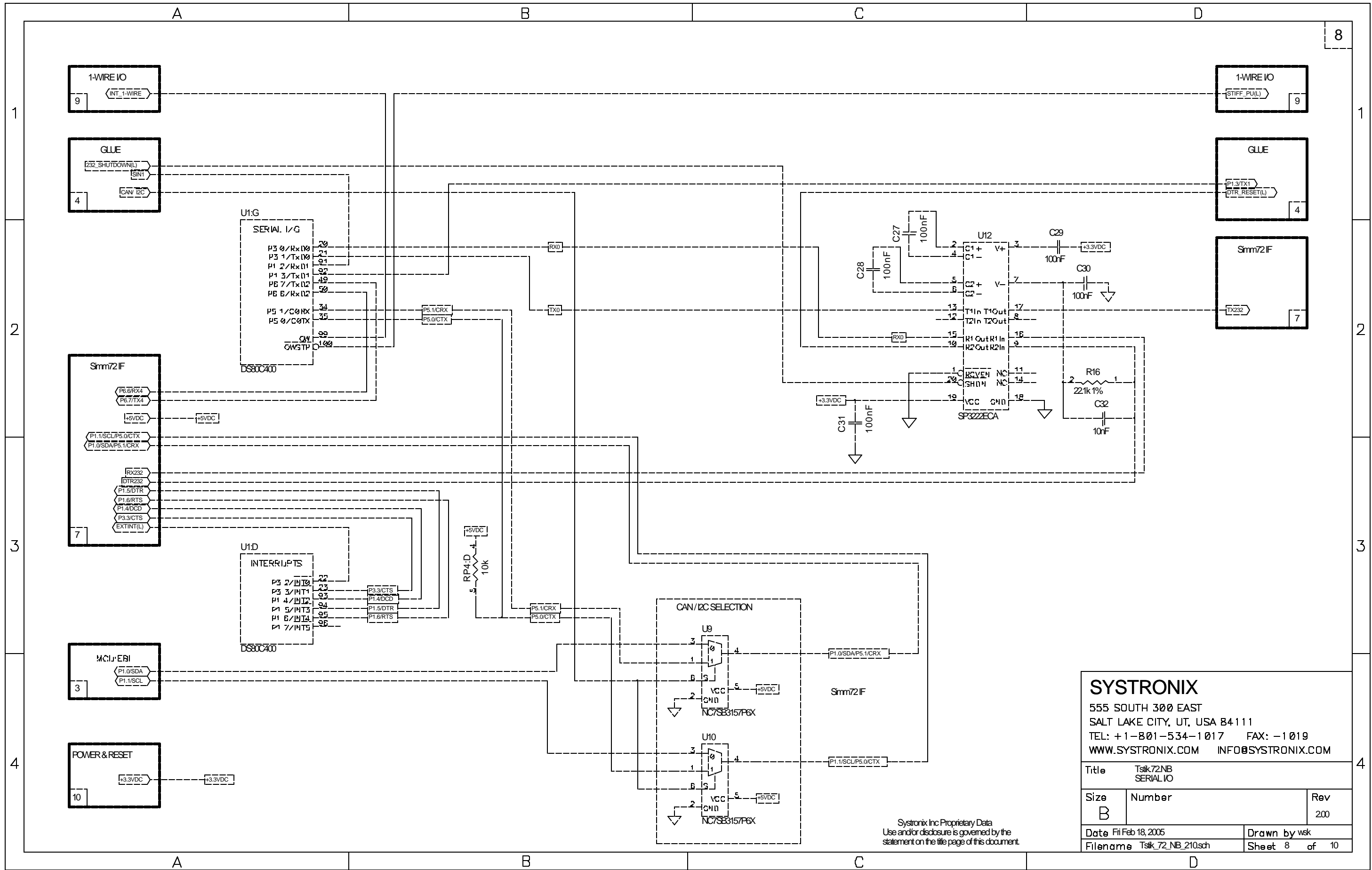
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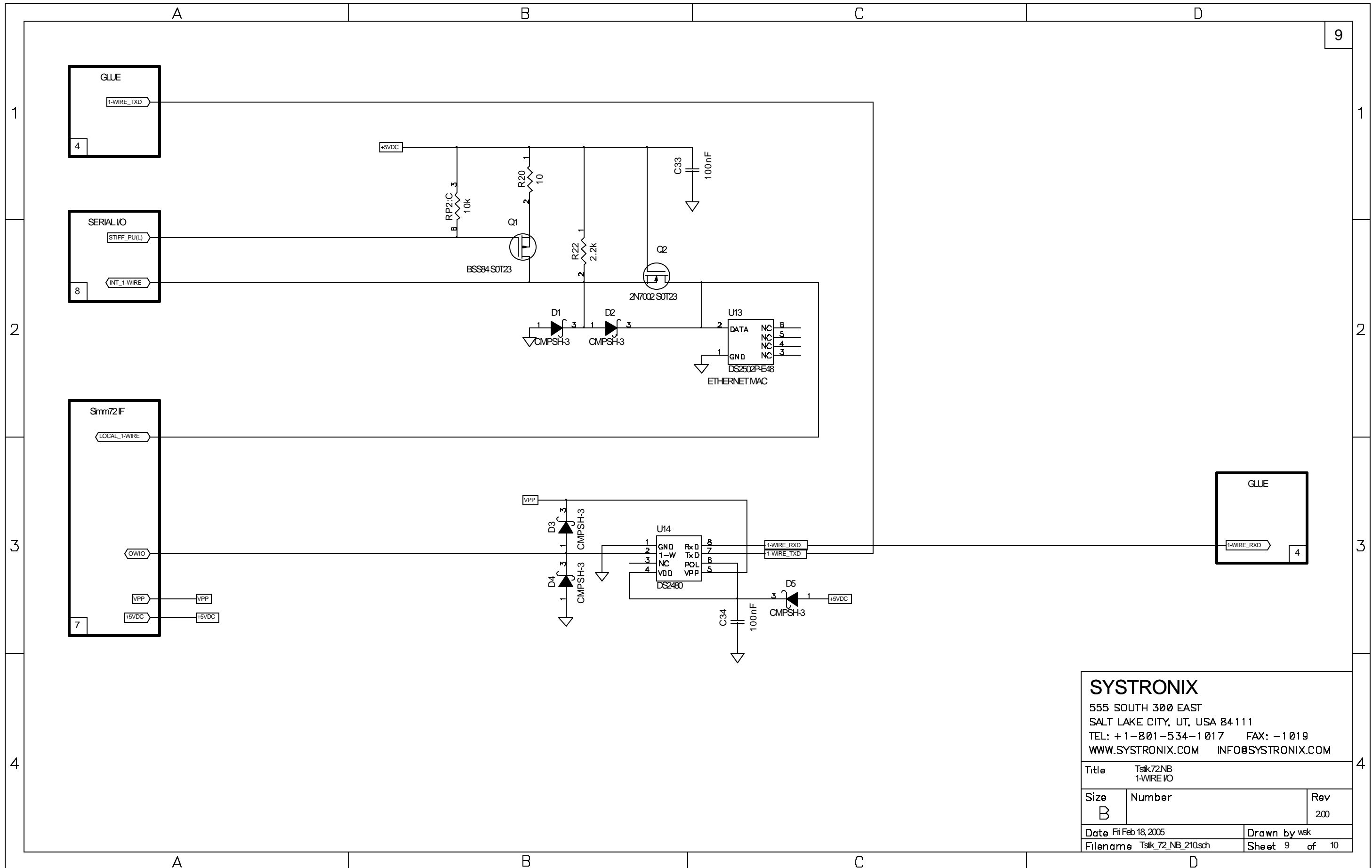
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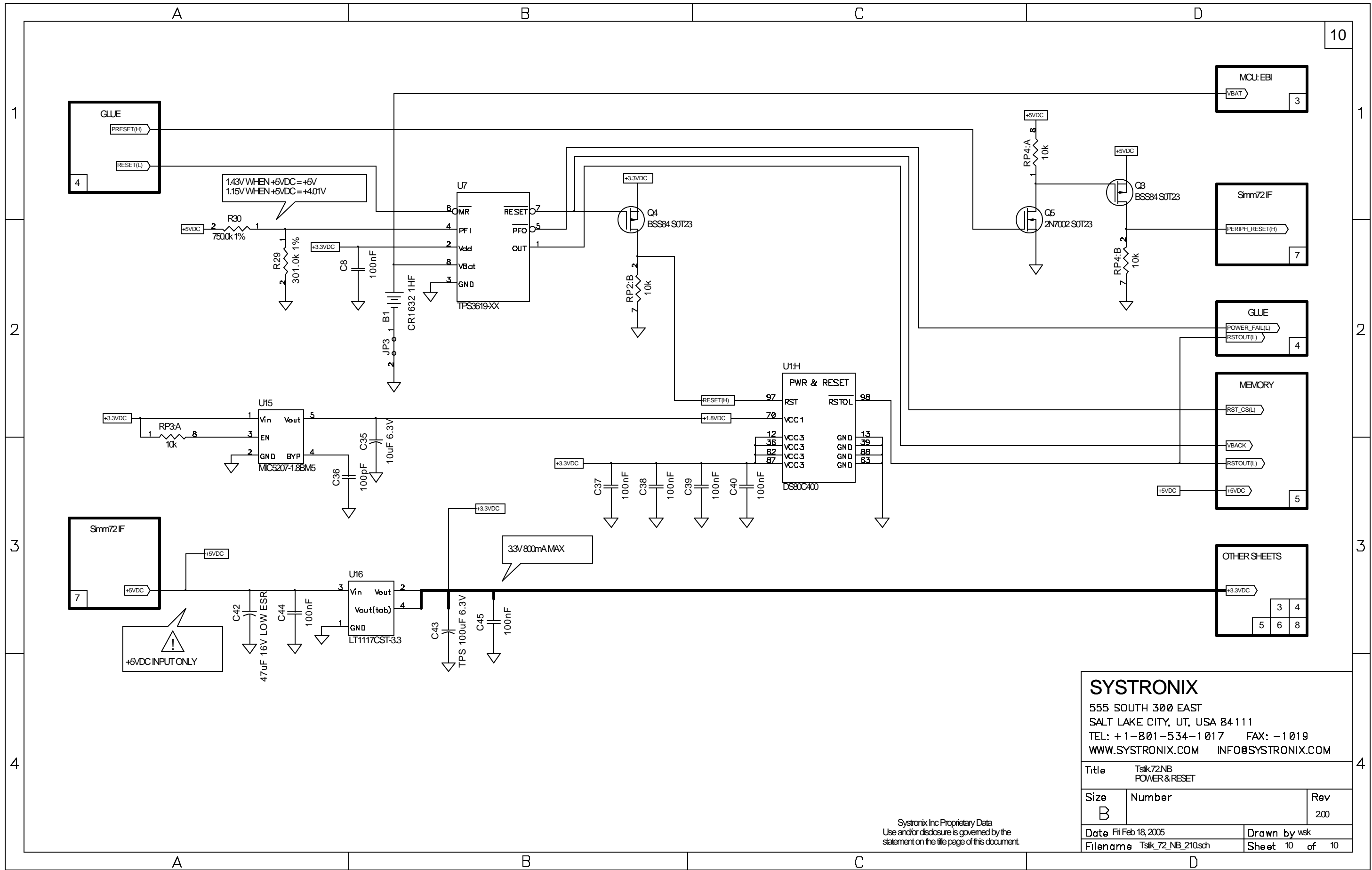
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