

TILT.400 – REVISIONS

SCH REV	PCB REV	DATE	BY	DESCRIPTION	SCH REV	PCB REV	DATE	BY	DESCRIPTION
0.0		02 DEC 31	wsk	START	3.10	3.10	06 AUG 31	wsk	Sheet 3: Added note at P4; Sheet 5: Added JP2, RP2; Sheet 6: Labeled P5 NNS;
0.01		03 JAN 23	wsk	Sheet 2: Added notes and Jumper table; Sheet 3: Modified M1 pin assignments (3-5); Added JP17,RP3;	3.20	3.20	06 OCT 17	wsk	Sheet 2: Corrected Jumpers Table; Sheet 3: Added JP24;
1.00	1.00	03 JAN 27	wsk	Sheet 7: Changed Reference Designators P4 & P6 to J/P1A & J/P1B;	3.21	3.20	06 DEC 01	wsk	Sheet 2: Modified Supported Features Table; Sheet 6: Changed part numbering for U9;
2.00	2.00	03 MAY 12	wsk	Sheet 3: Added P4; Sheet 5: Changed C19 to B size package; Changed U5 to SO8 package; Added P4; Sheet 7: Swapped J/P1A & J/P1B; Sheet 8: Changed C14 to 0603 package;	3.22	3.20	07 DEC 08	wsk	Sheet 2: Corrected JUMPERS Table (JP24);
2.10	2.10	03 JUL 16	wsk	PCB: Corrected wiring error at serial 0 / serial 4;					
2.11	2.10	03 SEP 26	wsk	Sheet 6: Replaced missing intersheet connector;					
2.12	2.10	03 OCT 14	wsk	Sheet 2: Corrected Note 5;					
2.12	2.11	03 NOV 18	wsk	PCB: Added rubber foot mounting locators to bottom silkscreen;					
2.13	2.11	03 DEC 10	wsk	Sheet 5: Changed C19 to 16V;					
2.14	2.11	04 JUL 26	wsk	Sheet 2: Added Note 6; Sheet 3: Added Embedlet Connector annotation; Sheet 4: Corrected JSimm / SimmStick Connector definition; Added note; Sheet 5: Corrected U7 component type; Sheet 6: Renamed this sheet; Marked C20, C21, & U15 as NOT NORMALLY STUFFED; Corrected intersheet reference; Added Device Code table;					
3.00	3.00	05 JAN 26	wsk	Sheet 2: Modified Notes and the Jumpers Table; Sheet 3: Connected TX1, XRX1, SDA, SCL to the M1; Added JP18-JP23 Sheet 4: Deleted C15, JP1, R2, RP1, RP2, U1, U2, U3 & U4; Added U1; Sheet 5: Deleted JP2, R3, U6, U8; Sheet 6: Deleted JP9, JP14, U13 & U16; Sheet 7: Added C22-C25, JP1, R2, U2; Sheet 8: Deleted P11;					
3.01	3.00	05 JUN 16	wsk	Sheet 7: Corrected Serial 1 Note; PCB: Corrected JP1 & JP6 labels;					
3.02	3.00	05 SEP 23	wsk	Sheet 2: Added JP2 & JP9 to Jumpers Table;					
3.03	3.00	05 DEC 23	wsk	Sheet 6: Added Note at P5;					

3

Systronix Inc Proprietary Information.
 This document contains financial, business, scientific, technical, economic or engineering information subject to USC § 1831-1839, Protection of Trade Secrets. Disclosure to others, use, or copying, without the express written authorization of Systronix Inc is strictly prohibited. Violation may result in criminal prosecution under 18 USC § 1831-1839 or 18 USC 1905.
 Copyright 1999, Systronix Inc.
 Unpublished Work. All rights reserved.

TABLE OF CONTENTS

SHEET	TITLE
1	REVISIONS
2	NOTES
3	Simm72 INTERFACE
4	JSimm INTERFACE
5	NETWORK I/O
6	1-WIRE I/O
7	SERIAL I/O
8	POWER & RESET

TO DO:

SYSTRONIX
 555 SOUTH 300 EAST
 SALT LAKE CITY, UT, USA 84111
 TEL: +1-801-534-1017 FAX: -1019
 WWW.SYSTRONIX.COM INFO@SYSTRONIX.COM

Title TILT.400 REVISIONS	
Size B	Rev 3.04
Date Mon Jan 08, 2007	Drawn by wsk
Filename TILT_400_322.sch	Sheet 1 of 8

JUMPERS			
JUMPER	CONDITION	DESCRIPTION	SHEET
JP1	SHORTED	DISABLES (TRI-STATES) SERIAL 1 RS-232 TRANSCEIVER	7
	6 OPEN	ENABLES SERIAL 1 RS-232 TRANSCEIVER	
JP2	1-2	I2C NET PULL-UP TO +5VDC	5
	2-3	I2C NET PULL-UP TO +3.3VDC	
JP3	SHORTED	TERMINATES CAN BUS	5
JP4	SHORTED	CONNECTS VRAW TO CAN BUS. CAN BUS MAY SOURCE RECIEVE POWER THROUGH THIS JPR. NOTE ON SH 5.	
⚠			
JP5	SHORTED	ASSERTION OF SERIAL 0 DTR CAUSES TStik RESET WHEN INSTALLED	7
JP6	SHORTED	DISABLES (TRI-STATES) SERIAL 4 RS-232 TRANSCEIVER	
4 JP6	OPEN	ENABLES SERIAL 4 RS-232 TRANSCEIVER	
JP7	NC PASTE*	FOR MANUFACTURING USE ONLY	8
JP8	1-2	CONNECTS +5VDC TO VPP. REQUIRED IF JP16 IS OPEN.	6
	2-3	CONNECTS +12VDC TO VPP. JP16 MUST BE OPEN.	
⚠ 3			
JP9		DELETED AT REV 3.00	
JP10	-	CONTROLS CAN TRANCEIVER MODE. SEE NOTE ON SHEET 5.	5
JP11	NC PASTE*	FOR MANUFACUTURING USE ONLY	
JP12	SHORTED	CONNECTS EXTERNAL 1-WIRE TO U9. OPEN THIS JUMPER WHEN JP8 PINS 2-3 ARE CLOSED.	6
	⚠ 3		
JP13	-	FOR MANUFACUTURING USE ONLY	
JP14		DELETED AT REV 3.00	
JP15	NC PASTE*	PARALLELS JP10 1-2. CONTROLS CAN TRANSCEIVER MODE. SEE NOTE ON SHEET 5.	5
⚠			
JP16	NC PASTE*	PARALLELS JP8 1-2. CONNECTS +5VDC TO VPP. MUST BE OPEN WHEN JP8 2-3 IS SHORTED.	6
	⚠ 3		
JP17	OPEN	REQUIRED FOR DALLAS TINI-390. CONNECTS CE0 TO RCE0. SPI NOT AVAILABLE.	3
JP18/JP19	NC PASTE*	OPEN THESE JUMPERS WHEN I2C FUNCTIONALITY REQUIRED WITH IMSYS SNAP.	3
7			
JP20/JP21	NO	CLOSE THESE JUMPERS ONLY WHEN I2C FUNCTIONALITY REQUIRED WITH IMSYS SNAP.	3
7			
JP22/JP23	NC PASTE*	OPEN THESE JUMPERS WHEN I2C FUNCTIONALITY REQUIRED WITH IMSYS SNAP.	3
7			
JP24	NO PASTE*	WHEN CLOSED ENABLES THE 2480 1-WIRE TRANSCEIVER	3

* NC PASTE JUMPERS ARE SHORTED DURING MANUFACTURING. THESE JUMPERS MAY BE OPENED IN THE FIELD.

TILT400 REV 3.xx SUPPORTED FEATURES					
FEATURE	SUPPORTED MODULE				
	TStik1	TStik2	TINI390	SNAP A-C	SNAP D+
ETHERNET	X	X	X	X	X
1-WIRE	1	1	1	4	4
I2C		X		5	X
SPI	X	X	3	3	3
CAN	x	X	X	X	X
SERIAL0	X	X	X	X	X
SERIAL1	1	1	1	5	5
SERIAL4		X		4	4

1. SIMULTANEOUS SERIAL 1 / 1-WIRE COMMUNICATION NOT SUPPORTED
2. [DELETED]
3. DALLAS STANDARD SPI AVAILABLE ONLY ON THE JSimm CONNECTOR
4. SIMULTANEOUS SERIAL 4 / 1-WIRE COMMUNICATION NOT SUPPORTED
5. SIMULTANEOUS SERIAL 1 / I2C COMMUNICATION NOT SUPPORTED

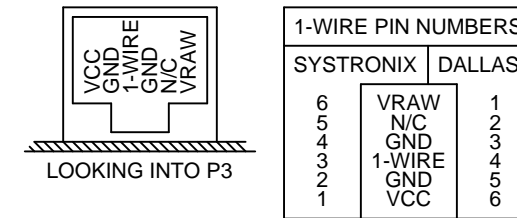
NOTES

- 1 JSimm pin definition is compliant with the SimmStick (TM) specification.
- ⚠ 2 SimmStick (TM) specification for pin 4 PWR, is 7.5 - 18Vdc.
- ⚠ 3 JP8 / JP16 SELECTS THE 1-WIRE PROGRAMMING VOLTAGE (VPP) SUPPLY SOURCE. C20, C21, JP8 & U15 ARE NOT STUFFED AT MANUFACTURING.

IF A PROGRAMMING VOLTAGE (VPP) IS REQUIRED, OPEN JP16 AND INSTALL C20, C21, JP8, & U15.

FOR NORMAL OPERATION INSTALL A SHORTING BLOCK AT JP8 PINS 1-2 TO CONNECT +5VDC TO THE TStik.72.NB DS2480 VPP PIN.

WHEN THE PROGRAMMING VOLTAGE IS REQUIRED INSTALL A SHORTING BLOCK AT JP8 PINS 2-3. OPEN JUMPER JP12 TO PROTECT U9 FROM VPP. BEFORE APPLYING VPP ENSURE THAT THE DEVICE IN S1 AND ANY DEVICES CONNECTED TO P3, P5 AND M2 (JSimm) ARE RATED FOR VPP. VPP MUST BE APPLIED TO THE SYSTEM BEFORE VCC.
- 4 SIGNAL CLASH MAY OCCUR IF U10 IS ENABLED WHEN ANOTHER DEVICE IS INSTALLED IN THE JSimm SOCKET (M2). CHECK THE JUMPERS JP6.
- 5 RJ-12 (P3) IS STANDARD DALLAS 1-WIRE ASSIGNMENT. DALLAS NUMBERS THE PINS DIFFERENTLY FROM RJ-12 MANUFACTURERS. REGARDLESS OF NUMBERING CONVENTION THE PHYSICAL LOCATION OF SIGNAL IS THE SAME ON DALLAS & SYSTRONIX BOARDS.



- 6 SIGNAL CLASH MAY OCCUR IF U17 IS ENABLED WHEN ANOTHER DEVICE IS INSTALLED IN THE JSimm SOCKET (M2). CHECK THE JUMPER JP1.
- 7 TILT400 SUPPORTS I2C FROM IMSYS SNAP ONLY ON SNAP SIMM72 PINS 14/15. FOR I2C FUNCTIONALITY WITH SNAP OPEN JP18, JP19, JP22, & JP23; CLOSE JP21 & JP22. WITH THIS CONFIGURATION SNAP SERIAL 1 FUNCTIONALITY IS NOT AVAILABLE.

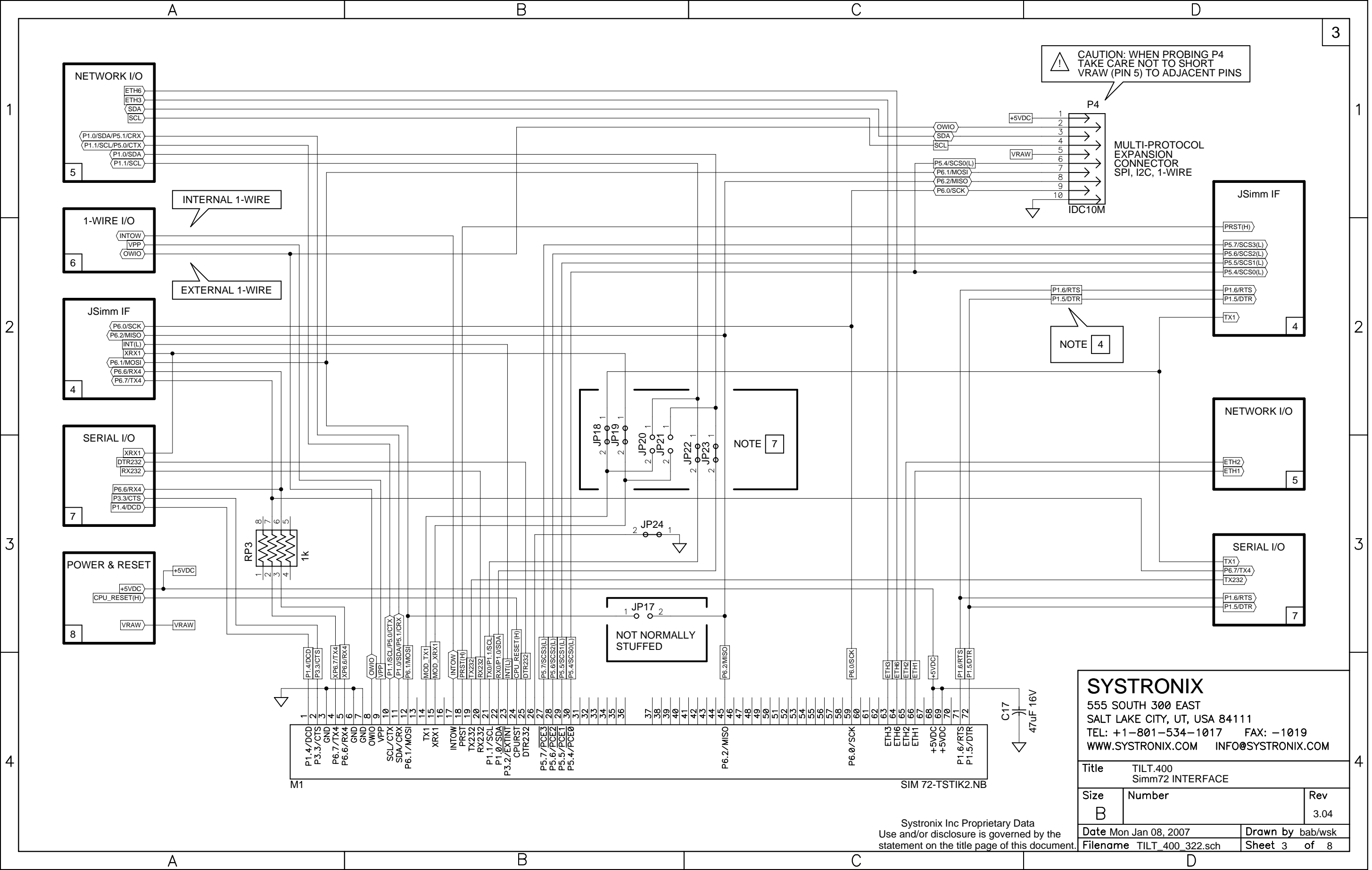
FOR NORMAL OPERATION WITH TStik2 CLOSE JP18, JP19, JP22, & JP23; OPEN JP20 & JP21.

SYSTRONIX

555 SOUTH 300 EAST
SALT LAKE CITY, UT, USA 84111
TEL: +1-801-534-1017 FAX: -1019
WWW.SYSTRONIX.COM INFO@SYSTRONIX.COM

Title	TILT.400 NOTES	
Size	Number	Rev
B		3.04
Date	Mon Jan 08, 2007	Drawn by wsk
Filename	TILT_400_322.sch	Sheet 2 of 8

Systronix Inc Proprietary Data
Use and/or disclosure is governed by the statement on the title page of this document.



CAUTION: WHEN PROBING P4 TAKE CARE NOT TO SHORT VRAW (PIN 5) TO ADJACENT PINS

MULTI-PROTOCOL EXPANSION CONNECTOR SPI, I2C, 1-WIRE

INTERNAL 1-WIRE

EXTERNAL 1-WIRE

NOTE 4

NOTE 7

JP17
1 2
NOT NORMALLY STUFFED

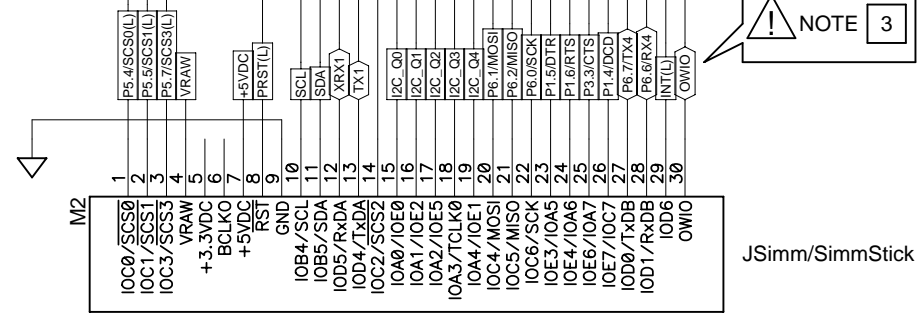
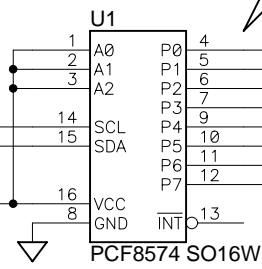
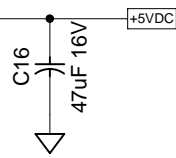
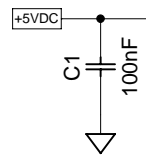
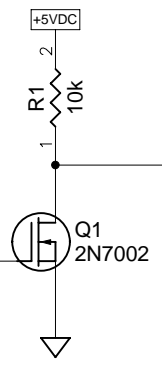
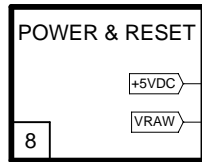
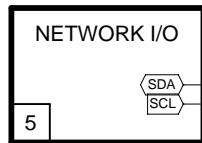
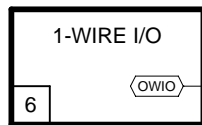
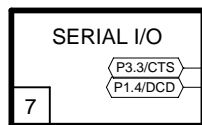
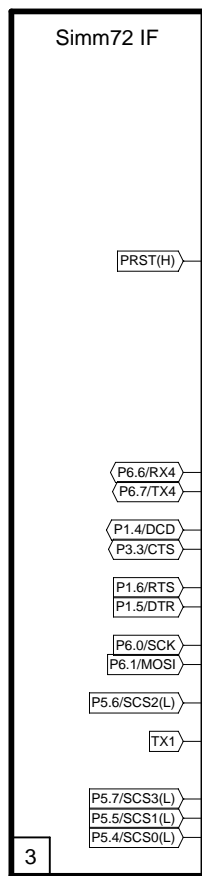
SYSTRONIX
555 SOUTH 300 EAST
SALT LAKE CITY, UT, USA 84111
TEL: +1-801-534-1017 FAX: -1019
WWW.SYSTRONIX.COM INFO@SYSTRONIX.COM

Title		TILT.400 Simm72 INTERFACE
Size	Number	Rev
B		3.04
Date	Mon Jan 08, 2007	Drawn by bab/wsk
Filename	TILT_400_322.sch	Sheet 3 of 8

Systronix Inc Proprietary Data
Use and/or disclosure is governed by the statement on the title page of this document.

I2C SLAVE ADDRESS = 0100111
 WRITING A '1' TO THIS REGISTER DRIVES THE CORRESPONDING OUTPUT HIGH.
 Iout @ Vout = 1V: 10mA typ, 25mA max
 Iout @ Vout = VCC: 30uA min, 300uA max

BYTE WIDE I/O AVAILABLE ON JSIMM PINS 15-22 IF SPI NOT IN USE.
 5 BITS OF I/O AVAILABLE ON JSIMM PINS 15-19 IF SPI IS IN USE



NOTE 2

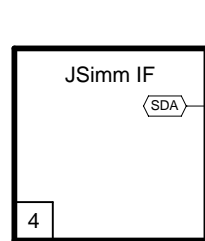
NOTE 3

NOTE 1

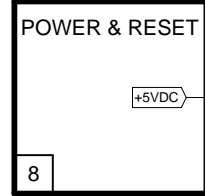
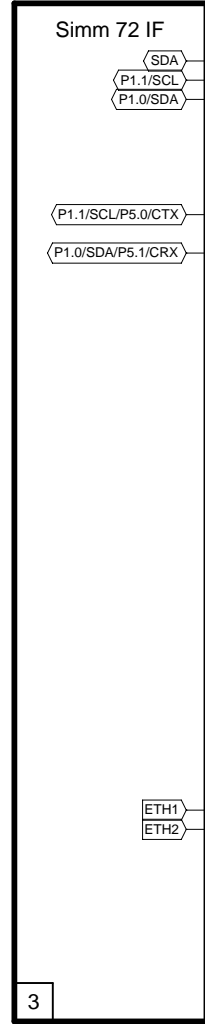
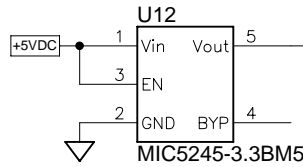
Systronix Inc Proprietary Data
 Use and/or disclosure is governed by the statement on the title page of this document.

SYSTRONIX
 555 SOUTH 300 EAST
 SALT LAKE CITY, UT, USA 84111
 TEL: +1-801-534-1017 FAX: -1019
 WWW.SYSTRONIX.COM INFO@SYSTRONIX.COM

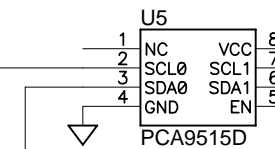
Title		TILT.400 JSimm INTERFACE
Size	Number	Rev
B		3.04
Date	Mon Jan 08, 2007	Drawn by bab/wsk
Filename	TILT_400_322.sch	Sheet 4 of 8



EXTERNAL I2C DATA

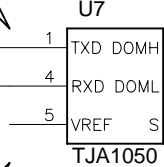


+5VDC



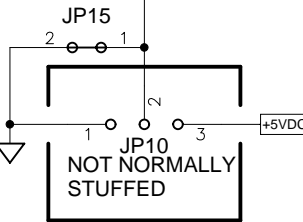
I2C BUFFER / REPEATER

ALTERNATE DEVICES: PCA82C250, PCA82C251 OK



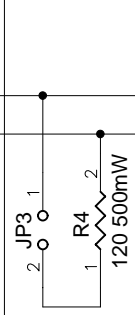
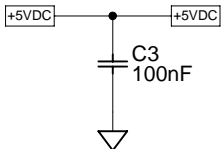
DEVICE @ U7	JP10*		MODE
	1-2	2-3	
TJA1050	OPEN SHORTED OPEN	OPEN OPEN SHORTED	HIGH SPEED HIGH SPEED LISTEN
PCA82C250/1	OPEN SHORTED OPEN	OPEN OPEN SHORTED	ILLEGAL HIGH SPEED SHUTDOWN

* JP16 OPEN. DO NOT SHORT JP10 PINS 2-3 WITH JP16 SHORTED.

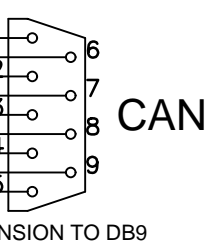
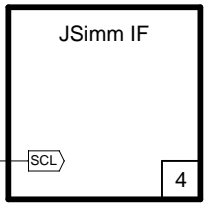


NOT NORMALLY STUFFED

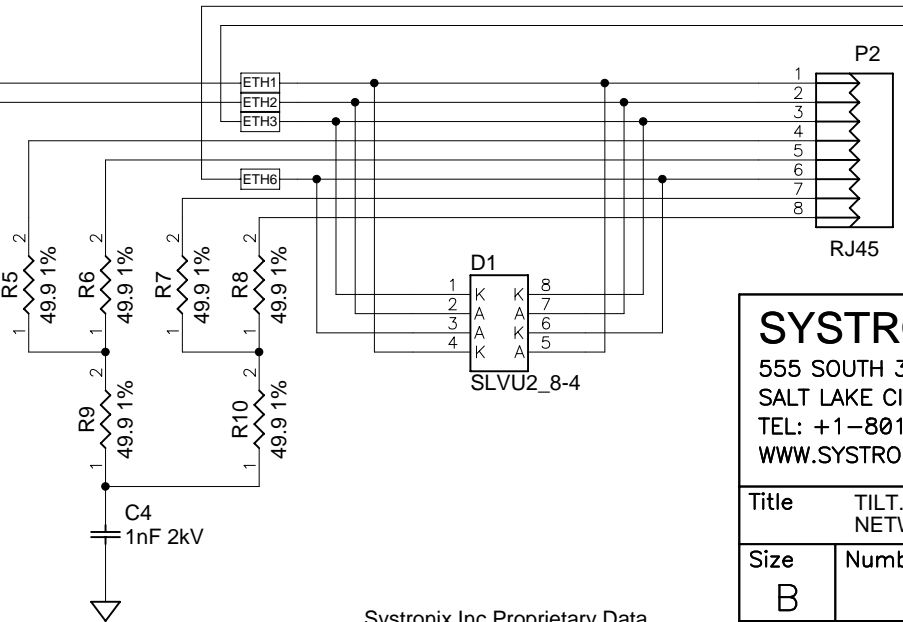
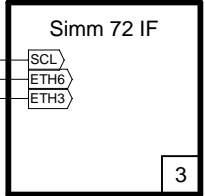
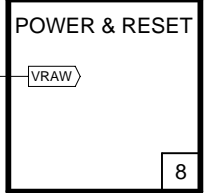
EXTERNAL I2C CLOCK



WHEN USED TO POWER THIS BOARD, VCAN+ MUST NOT EXCEED 24V.



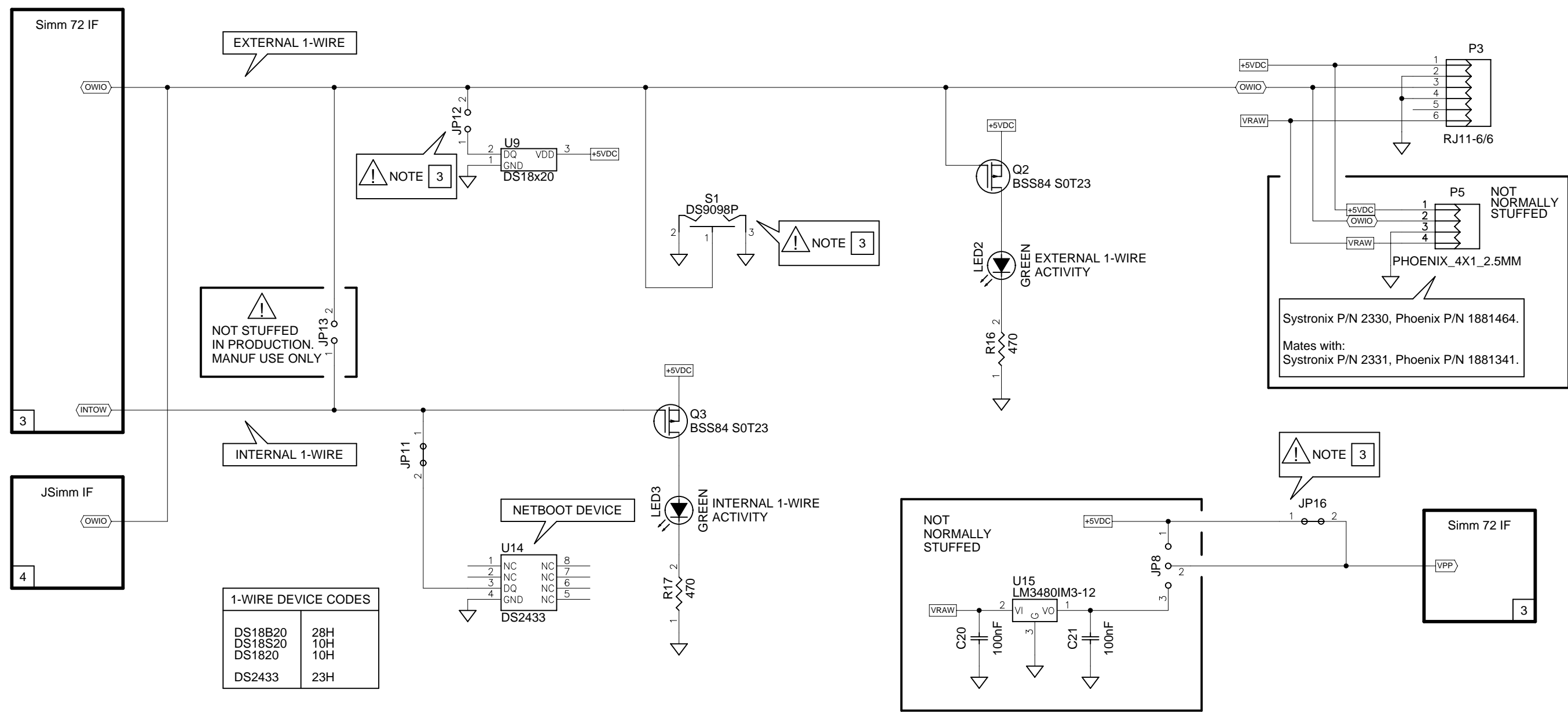
CAN



SYSTRONIX
 555 SOUTH 300 EAST
 SALT LAKE CITY, UT, USA 84111
 TEL: +1-801-534-1017 FAX: -1019
 WWW.SYSTRONIX.COM INFO@SYSTRONIX.COM

Title		TILT.400 NETWORK I/O
Size	Number	Rev
B		3.04
Date	Mon Jan 08, 2007	Drawn by bab/wsk
Filename	TILT_400_322.sch	Sheet 5 of 8

Systronix Inc Proprietary Data
 Use and/or disclosure is governed by the
 statement on the title page of this document.

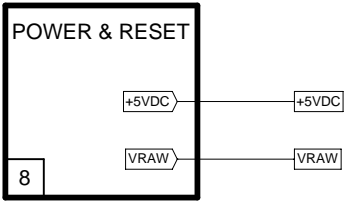


NOT STUFFED IN PRODUCTION. MANUF USE ONLY

NOTE 3

NOTE 3

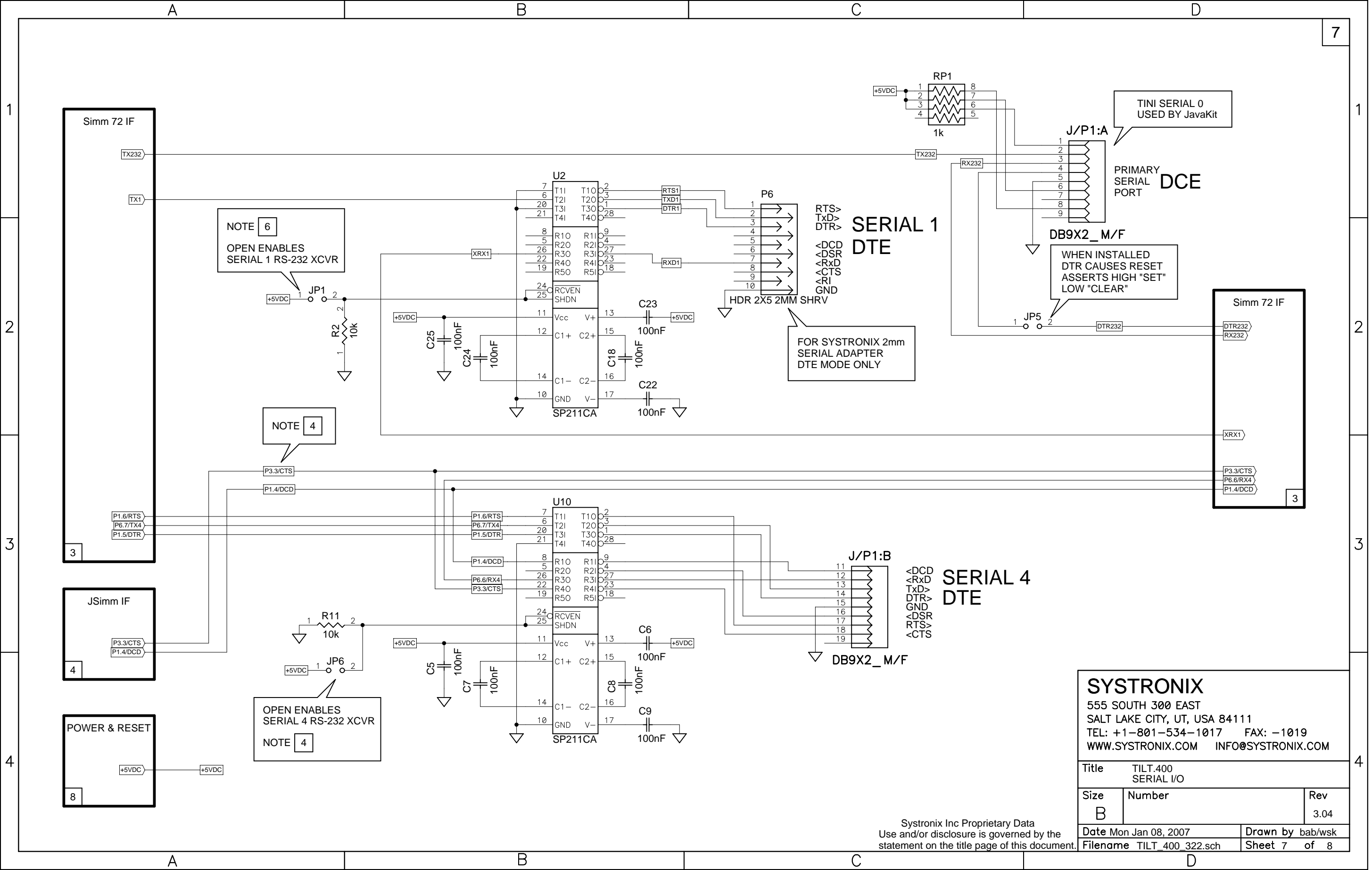
1-WIRE DEVICE CODES	
DS18B20	28H
DS18S20	10H
DS1820	10H
DS2433	23H



SYSTRONIX
 555 SOUTH 300 EAST
 SALT LAKE CITY, UT, USA 84111
 TEL: +1-801-534-1017 FAX: -1019
 WWW.SYSTRONIX.COM INFO@SYSTRONIX.COM

Title	TILT.400 1-WIRE I/O	
Size	Number	Rev
B		3.04
Date	Mon Jan 08, 2007	Drawn by bab/wsk
Filename	TILT_400_322.sch	Sheet 6 of 8

Systronix Inc Proprietary Data
 Use and/or disclosure is governed by the
 statement on the title page of this document.



NOTE 6
OPEN ENABLES
SERIAL 1 RS-232 XCVR

NOTE 4

OPEN ENABLES
SERIAL 4 RS-232 XCVR
NOTE 4

FOR SYSTRONIX 2mm
SERIAL ADAPTER
DTE MODE ONLY

TINI SERIAL 0
USED BY JavaKit

PRIMARY
SERIAL
PORT
DCE

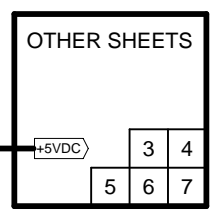
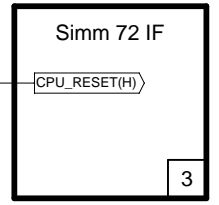
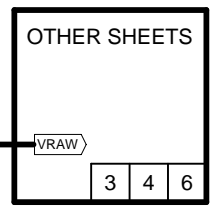
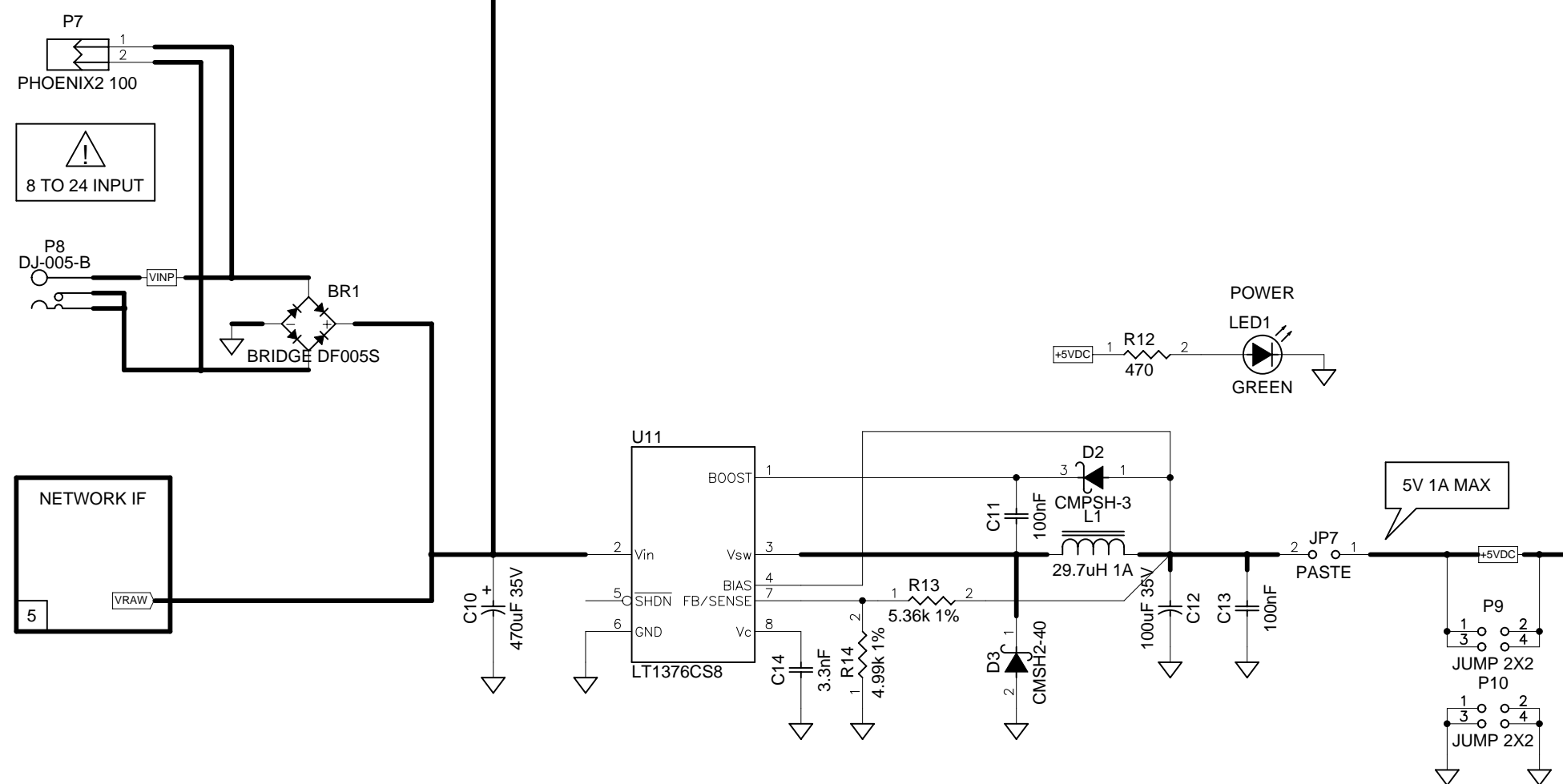
DB9X2_M/F
WHEN INSTALLED
DTR CAUSES RESET
ASSERTS HIGH "SET"
LOW "CLEAR"

SERIAL 4
DTE
<DCD
<RxD
TxD>
DTR>
GND
<DSR
RTS>
<CTS

SYSTRONIX
555 SOUTH 300 EAST
SALT LAKE CITY, UT, USA 84111
TEL: +1-801-534-1017 FAX: -1019
WWW.SYSTRONIX.COM INFO@SYSTRONIX.COM

Title		TILT.400 SERIAL I/O
Size	Number	Rev
B		3.04
Date	Mon Jan 08, 2007	Drawn by bab/wsk
Filename	TILT_400_322.sch	Sheet 7 of 8

Systronix Inc Proprietary Data
Use and/or disclosure is governed by the
statement on the title page of this document.



SYSTRONIX
 555 SOUTH 300 EAST
 SALT LAKE CITY, UT, USA 84111
 TEL: +1-801-534-1017 FAX: -1019
 WWW.SYSTRONIX.COM INFO@SYSTRONIX.COM

Title		TILT.400 POWER & RESET
Size	Number	Rev
B		3.04
Date	Mon Jan 08, 2007	Drawn by wsk
Filename	TILT_400_322.sch	Sheet 8 of 8

Systronix Inc Proprietary Data
 Use and/or disclosure is governed by the
 statement on the title page of this document.