

SYSTRONIX TINI ENGINEERING PLATFORM (STEP) – REVISIONS

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SCH REV	PCB REV	DATE	BY	DESCRIPTION	SCH REV	DATE	BY
0.0		00 Jan 13	wsk	Start of schematic capture.			
0.1		00 Jan 20	wsk	Initial schematic capture complete.			
1	1	00 Jan 27	wsk	Changed name to Systronix TINI Evaluation Platform (STEP); Added descriptions to Notes page;			
2	2	00 May 30	wsk	Sheet 3: Changed TINI module to 68/72 pin device; Connected all wires between TINI module and spare module; Connected OWRTN to ground; Added IrDA support; renamed INTOW to INTOW/IRDACK; Sheet 6: Deleted C6, P3, P5, R8; Sheet 7: Connected OWRTN to ground; Deleted DS2401 added DS2502; Deleted C9-C14, D1, J3, JP4, P8, Q1, R11, RP1, & U5; Added IrDA support, C6, C9, C10, R8, U5, & U11; Sheet 9: Added C27; Deleted JP8; Added IrDA support;			
2.1	2.1	00 Jun 01	wsk	Sheet 2: Updated notes page; Sheet 5: Renamed JP2 to P3; Moved ROM select signal from U2-19 to U2-18; Changed R5 & R6 to 470 ohm; Sheet 6: Added JP10; Changed U4 to 74HCT14; Renamed JP3 to JP8; Sheet 7: Inserted U4A & B in the signal path to buffer the IrDA clock; Renamed JP4 to JP3; Renamed JP8 to JP4; Renamed P6 to P5; Renamed P7 to P6; Renamed J6 to P12; Sheet 9: Renamed JP9 to JP2; Renamed JP10 to JP9; Renamed P12 to P7; Renamed P13 to P8; Added P13;			
2.11	2.1	00 Aug 21	wsk	Sheet 1: Minor formatting changes; Sheet 2: Minor corrections to the Notes;			

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TO DO:

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Title SYSTRONIX TINI ENGINEERING PLATFORM (STEP)
REVISIONS

Size	Number	Rev
B		2.1

Date Mon Aug 21, 2000 Drawn by wsk
Filename Step_021.sch Sheet 1 of 9

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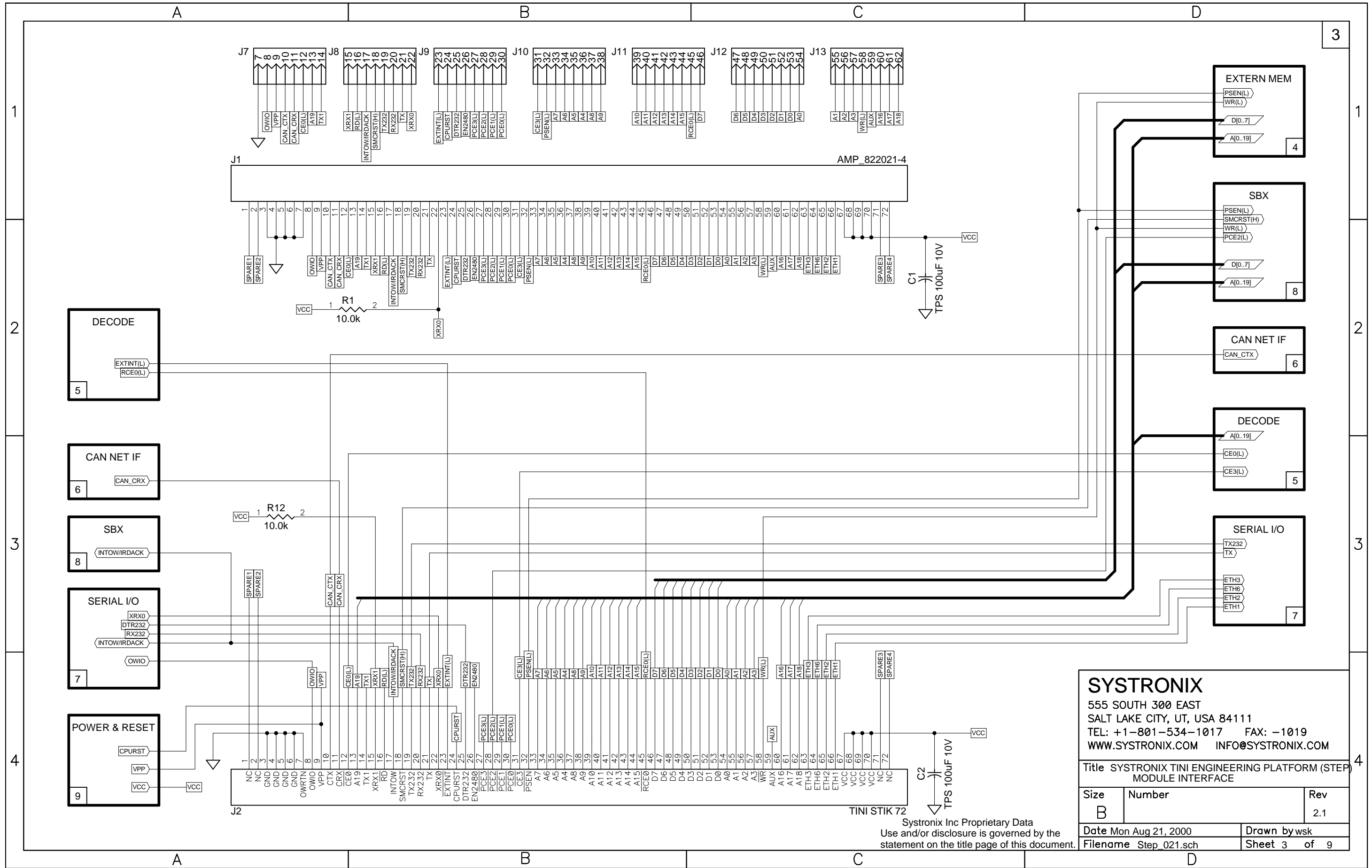
A

B

C

D

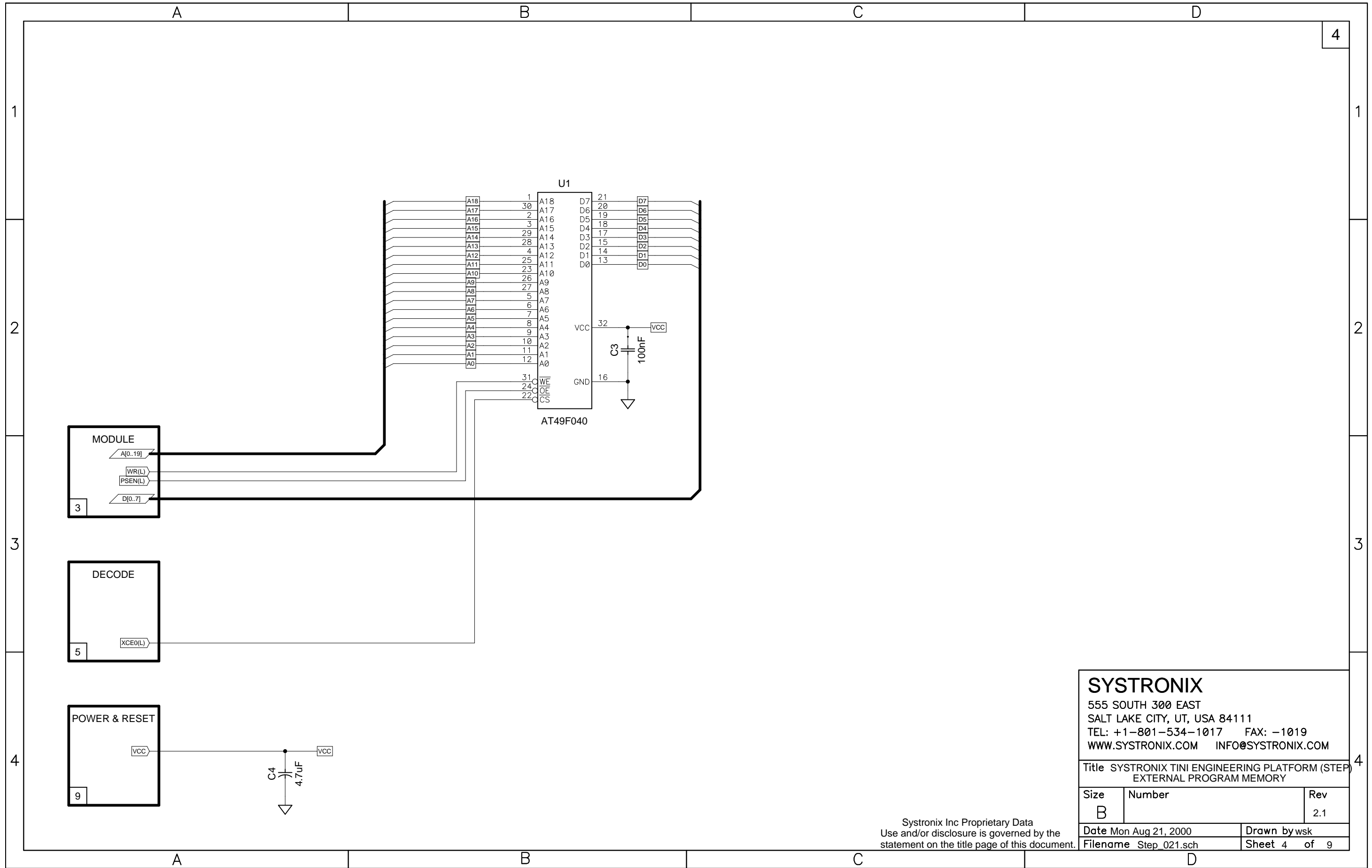
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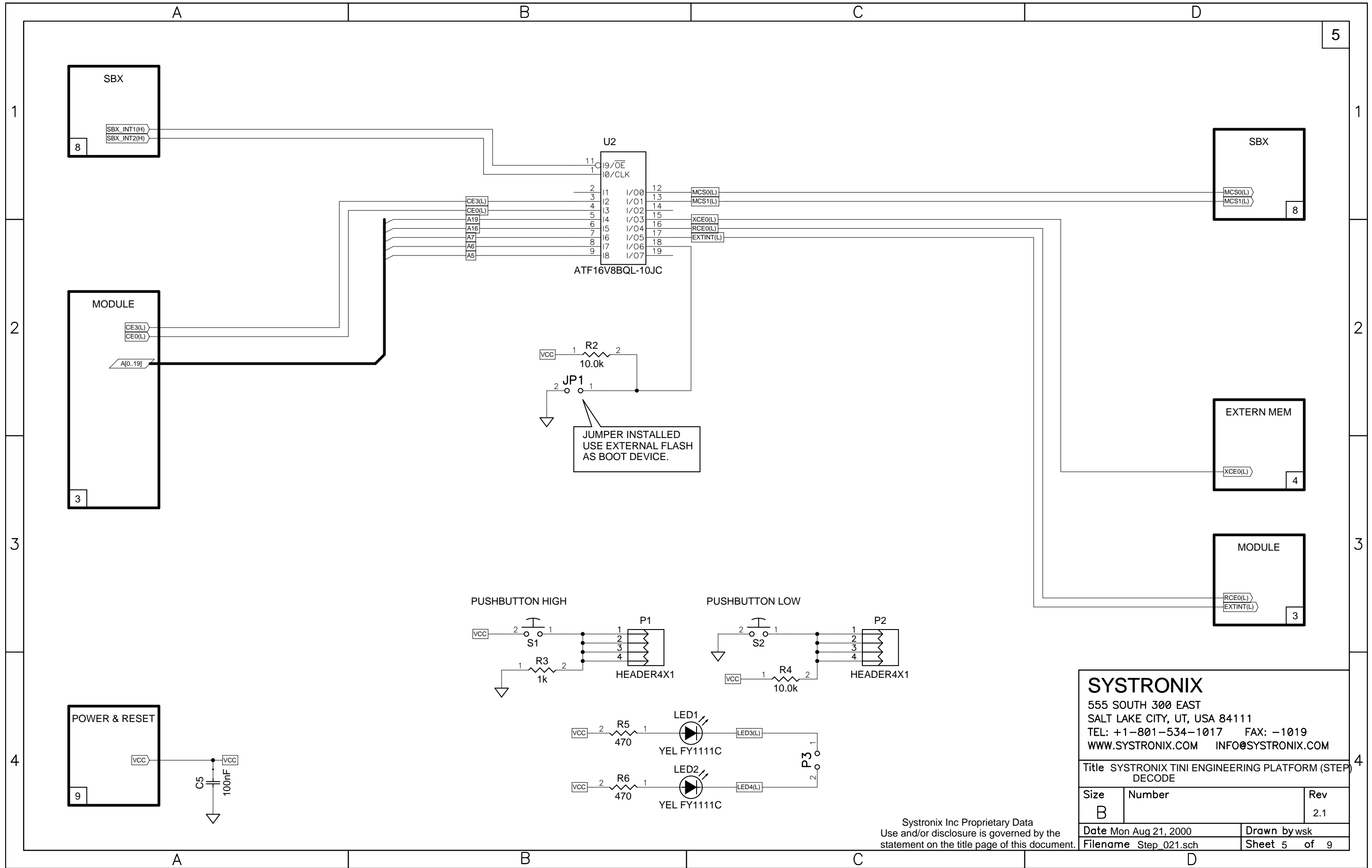
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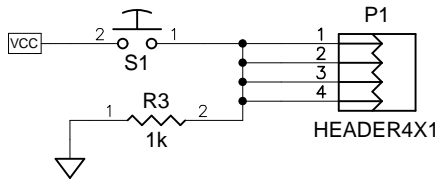
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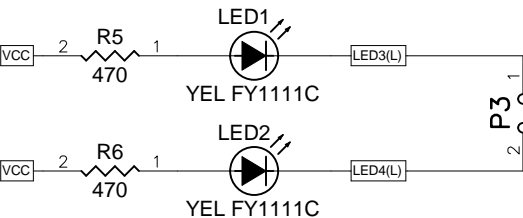
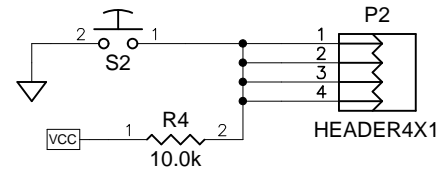


JUMPER INSTALLED
USE EXTERNAL FLASH
AS BOOT DEVICE.

PUSHBUTTON HIGH

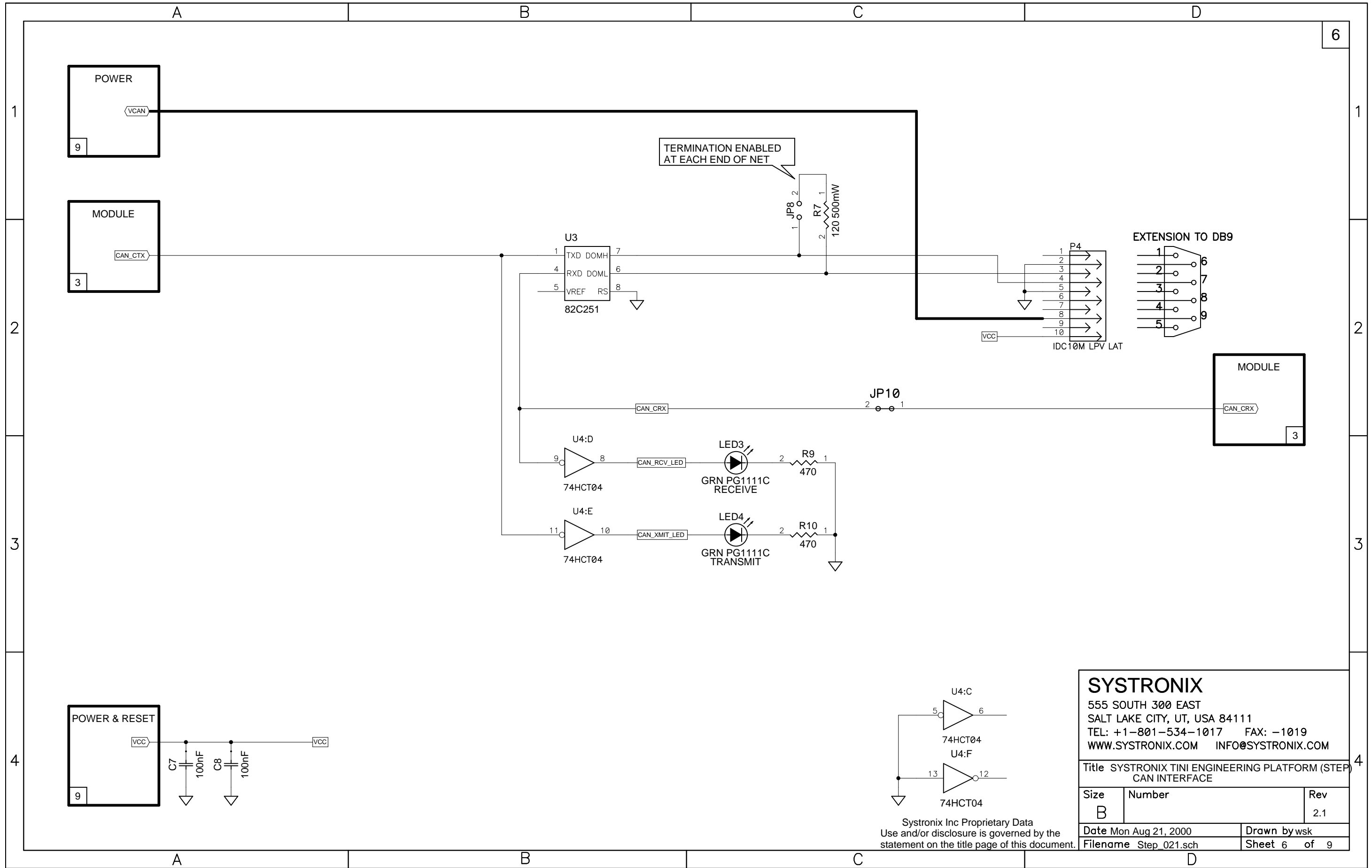


PUSHBUTTON LOW



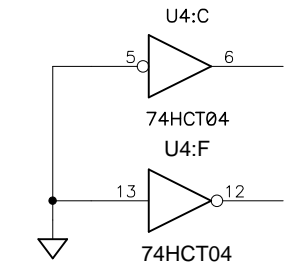
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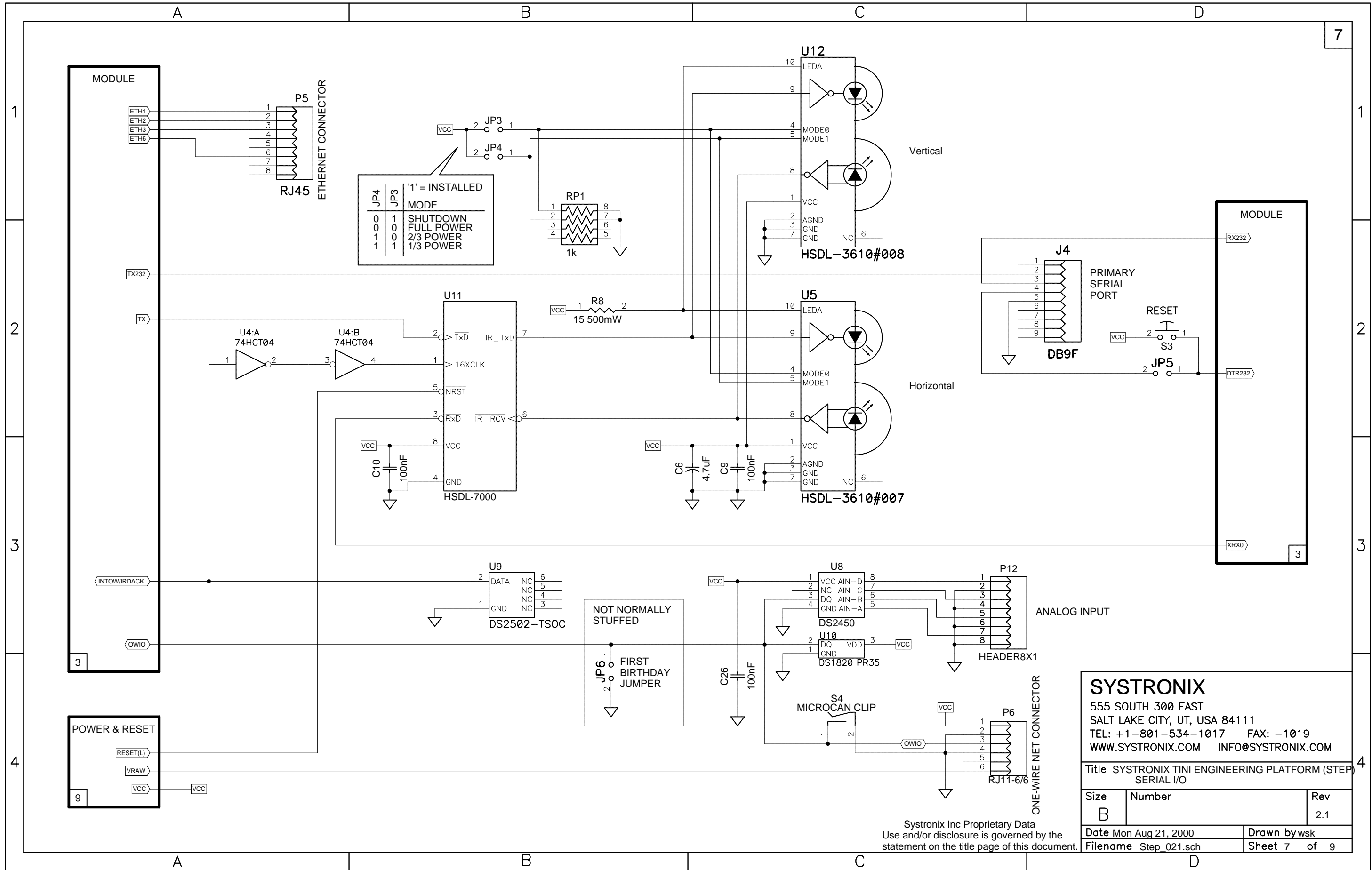


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Title SYSTRONIX TINI ENGINEERING PLATFORM (STEP 6) CAN INTERFACE		
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JP4	JP3	'1' = INSTALLED	MODE
0	0	1	SHUTDOWN
0	1	0	FULL POWER
1	0	0	2/3 POWER
1	1	1	1/3 POWER

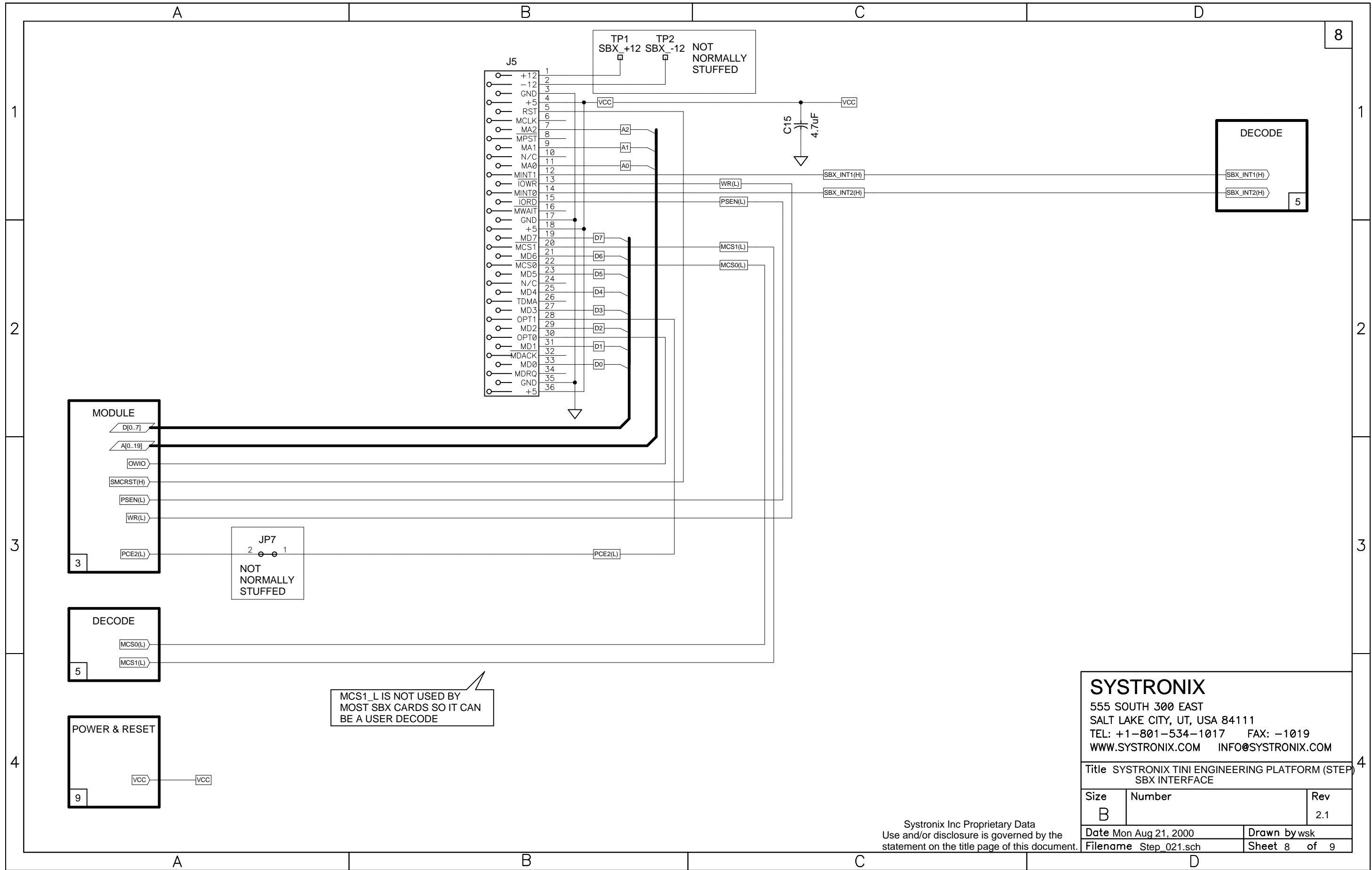
NOT NORMALLY STUFFED

JP6
1
2
FIRST BIRTHDAY JUMPER

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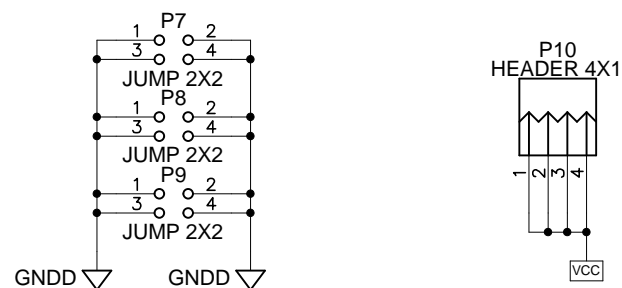
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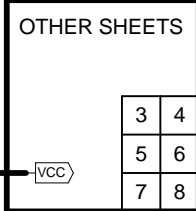
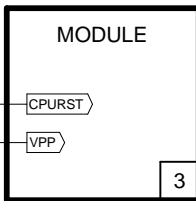
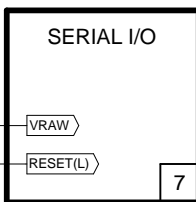
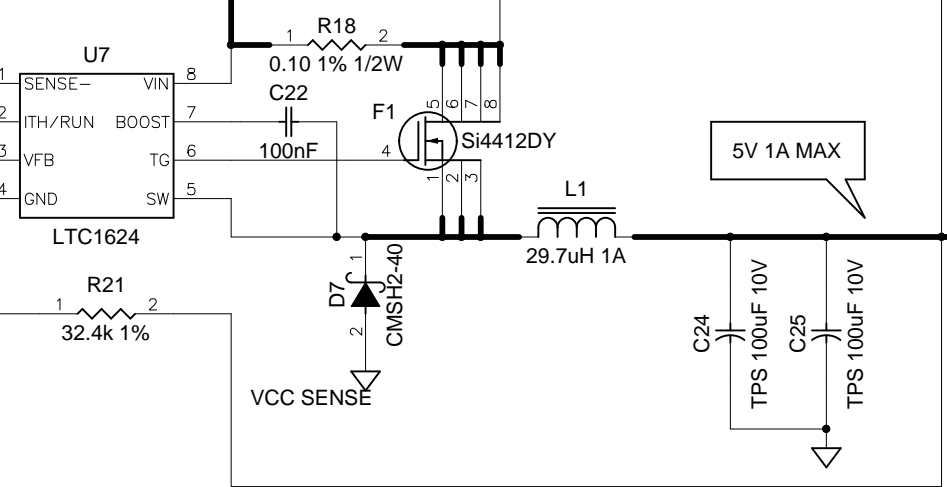
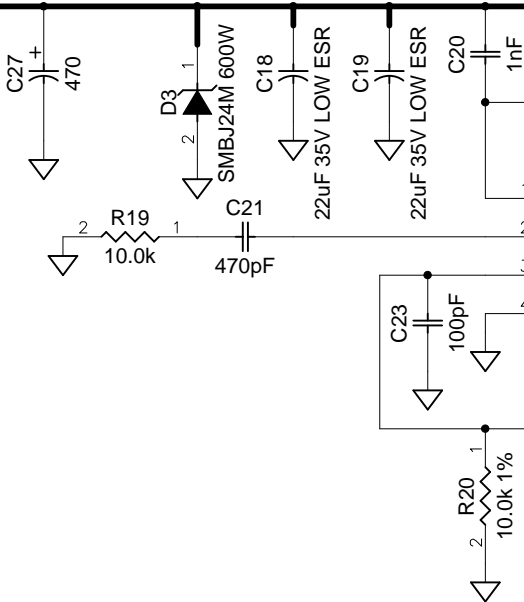
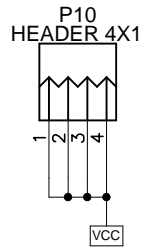
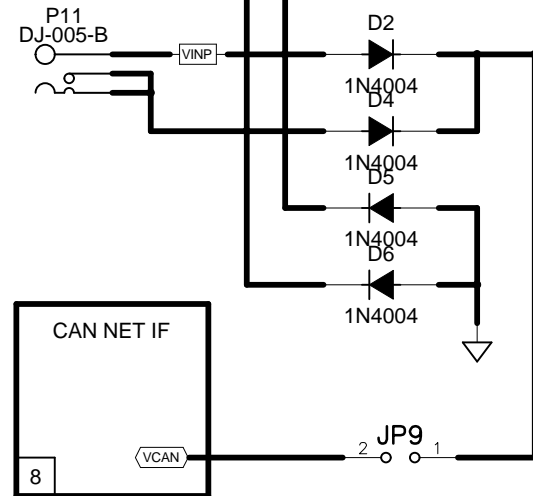
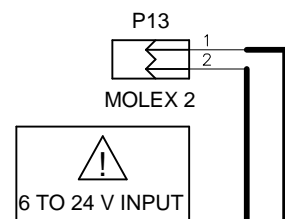
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Title SYSTRONIX TINI ENGINEERING PLATFORM (STEP 4) SBX INTERFACE		
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DIGITAL SUPPLY TEST POINTS



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Title SYSTRONIX TINI ENGINEERING PLATFORM (STEP POWER)		
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