

SAJE: Systronix aJile EuroBoard – REVISIONS

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SCH REV	PCB REV	DATE	BY	DESCRIPTION	PCB REV	DATE	BY	
0.0		01 JAN 05	wsk	START	1.0	01 JAN 30	wsk	PCB Rev 1 done.
1.0	1.0	01 JAN 30	wsk	PCB Rev 1 done.	2.0	01 APR 30	wsk	Voided ground and power planes under ethernet termination networks; Changed U6 to SOIC package; Added pin locator silk-screen ticks to fine-pitch devices; Changed U5, U21, & U22 to 74LVX3245 TSSOP;
1.01		01 FEB 02	wsk	Sheet 7: Changed CPLD from XC9536XL to XC9572XL;				
1.02		01 FEB 06	wsk	Sheet 8: Corrected data in/out connections between U6 & U23; Changed U6 from DIP to SOIC, type A to type B; Sheet 9: Changed U5, U21, & U22 to 74LVX3245 TSSOP; Sheet 13: Added R12 560k resistor across the crystal to assist oscillator startup;				
1.03		01 FEB 13	wsk	Sheet 13: Changed R12 to 1M; Changed C80 to 47pF;				
1.04		01 FEB 20	wsk	Sheet 3: Added WAIT(L); Sheet 7: Added WAIT(L), SBX_RD(L) & SBX_WR(L); Sheet 9: Disconnected SBX_RD(L) and SBX_WR(L) from U5;				
1.05		01 APR 02	wsk	Sheet 4: Changed C43 package size, changed C81, C82 value and package size; Sheet 5: Changed C16, C17, C19 value and package size; Sheet 6: Changed C18 value and package size; Sheet 6: Changed C83 package size;				
1.06		01 APR 03	wsk	Sheet 3: Deleted P7; Added C1, JP8, R16, U24 & U25; Removed RE(L) & WE(L) connection to Sheet 9;  Sheet 7: Deleted GND, TCK, TDI, TDO, TMS, TP5, TP10, TP11, VCC; Sheet 9: Removed RE(L) & WE(L); Change U5, U21, & U22 to 74LVC4245A; Sheet 9: Renamed P2 & P3 to J7 & J9; Renamed P6 to JP10; Sheet 10: Renamed P8 to J2; Sheet 11: Renamed S1 to SW2; Deleted C79, JP7, MCU_GND, MCU_TCK, MCU_TDI, MCU_TDO, MCU_TMS, MCU_TRST, RP3, U3; Added C2, R17, R18;				
2.00	2.0	01 APR 30	wsk	PCB Rev 2 done				
2.01	2.0	01 JUL 20	wsk	Sheet 2: Added notes and jumper descriptions;				

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Title	SAJE: Systronix aJile Java Euroboard REVISIONS	
Size	Number	Rev
B		1.06
Date	Fri Jul 20, 2001	Drawn by wsk
Filename	SAJE_201.sch	Sheet 1 of 13

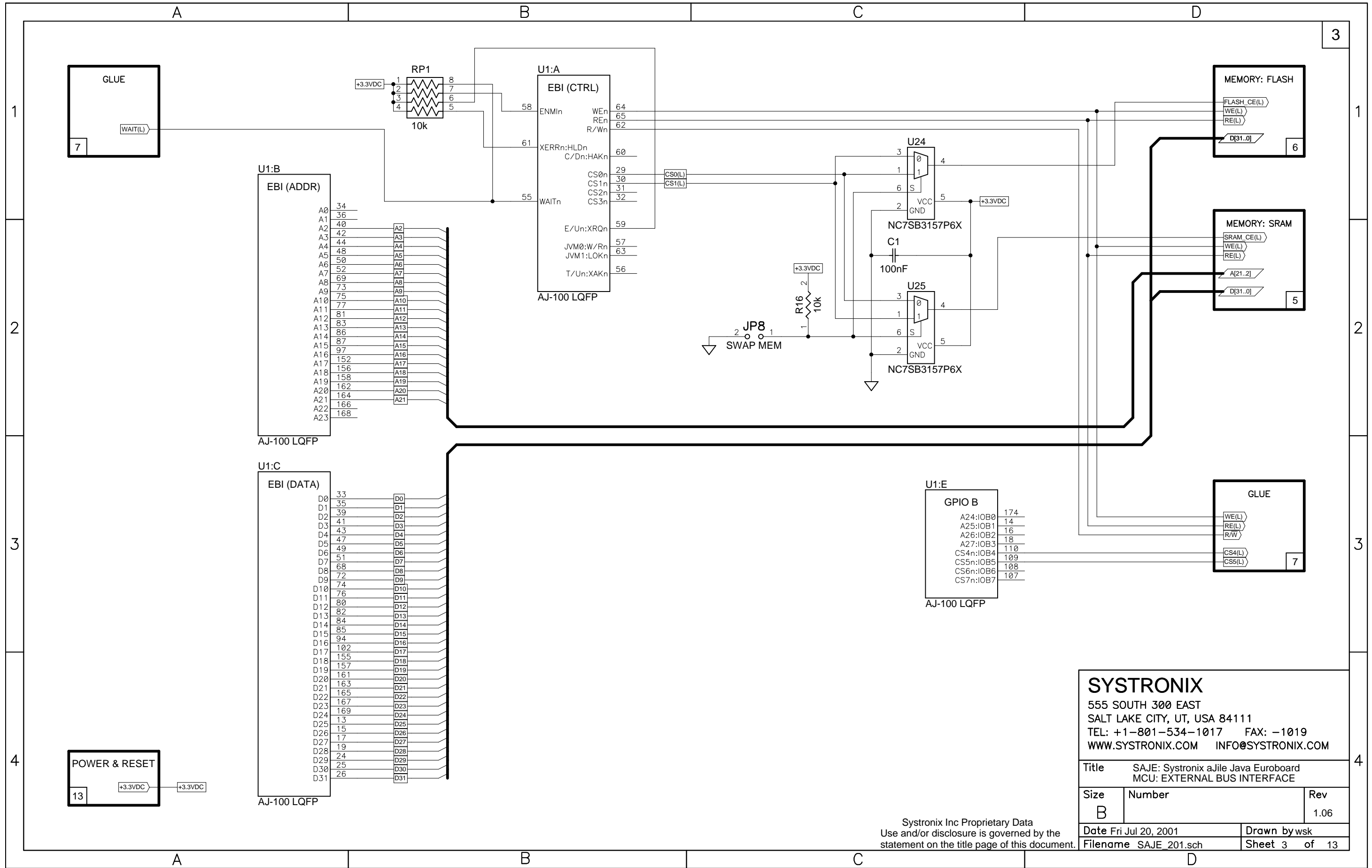
4

		A		B		C		D		2		
1	JP1	NO USER OPTION. SELECTS POWER SUPPLY FOR U2 & U13						SHEET 12				
	JP2	1-2	UART 1 TxD TO RS-232 TRANSCEIVER U2						SHEET 12			
		2-3	UART 1 TxD TO DALLAS 1-WIRE TRANSCEIVER U14									
	JP3	NO USER OPTION. ISOLATES THE +5VDC REGULATOR						SHEET 13				
	JP4	1-2	UART 1 RxD FROM RS-232 TRANSCEIVER U2						SHEET 12			
		2-3	UART 1 RxD FROM DALLAS 1-WIRE TRANSCEIVER U14									
JP5	NO USER OPTION. ISOLATES THE +3.3VDC REGULATOR						SHEET 13					
JP6	1-2	JTAG PORT COMMUNICATES WITH CPLD U4						SHEET 11				
	2-3	JTAG PORT COMMUNICATES WITH aJ-100										
JP8	INSTALLED NOT INSTALLED	CS0(L)		CS1(L)				SHEET 3				
		SRAM_CE(L) FLASH_CE(L)		FLASH_CE(L) SRAM_CE(L)								
2	⚠	1-2	+5VDC TO THE DS2480 VPP PIN; SEE NOTE 1									
		2	VPP (+12) FOR 1-WIRE EPROM PROGRAMING						1		SHEET 10	
		3	RETURN (GND) FOR EXTERNAL VPP SUPPLY									
JP10	1-2	SW2 TO IOA3										
	3-4	SW2 TO IOA4										
	5-6	SW2 TO IOA5										
	7-8	SW2 TO IOA6								SHEET 11		
<p>1 JP9 PROVIDES AN ACCESS POINT FOR AN EXTERNAL PROGRAMMING VOLTAGE SUPPLY. IF EPROM PROGRAMMING IS NOT REQUIRED, A JUMPER MUST BE INSTALLED TO CONNECT +5VDC TO THE DS2480 VPP PIN. VPP MUST BE APPLIED BEFORE +5VDC.</p>												
<p>2 MCS0(L) address range 0x0140_0000 ... 0x0140_FFFF MCS1(L) address range 0x0141_0000 ... 0x0141_FFFF</p>												
3												
4												
		A		B		C		D		4		

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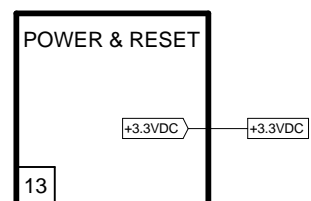
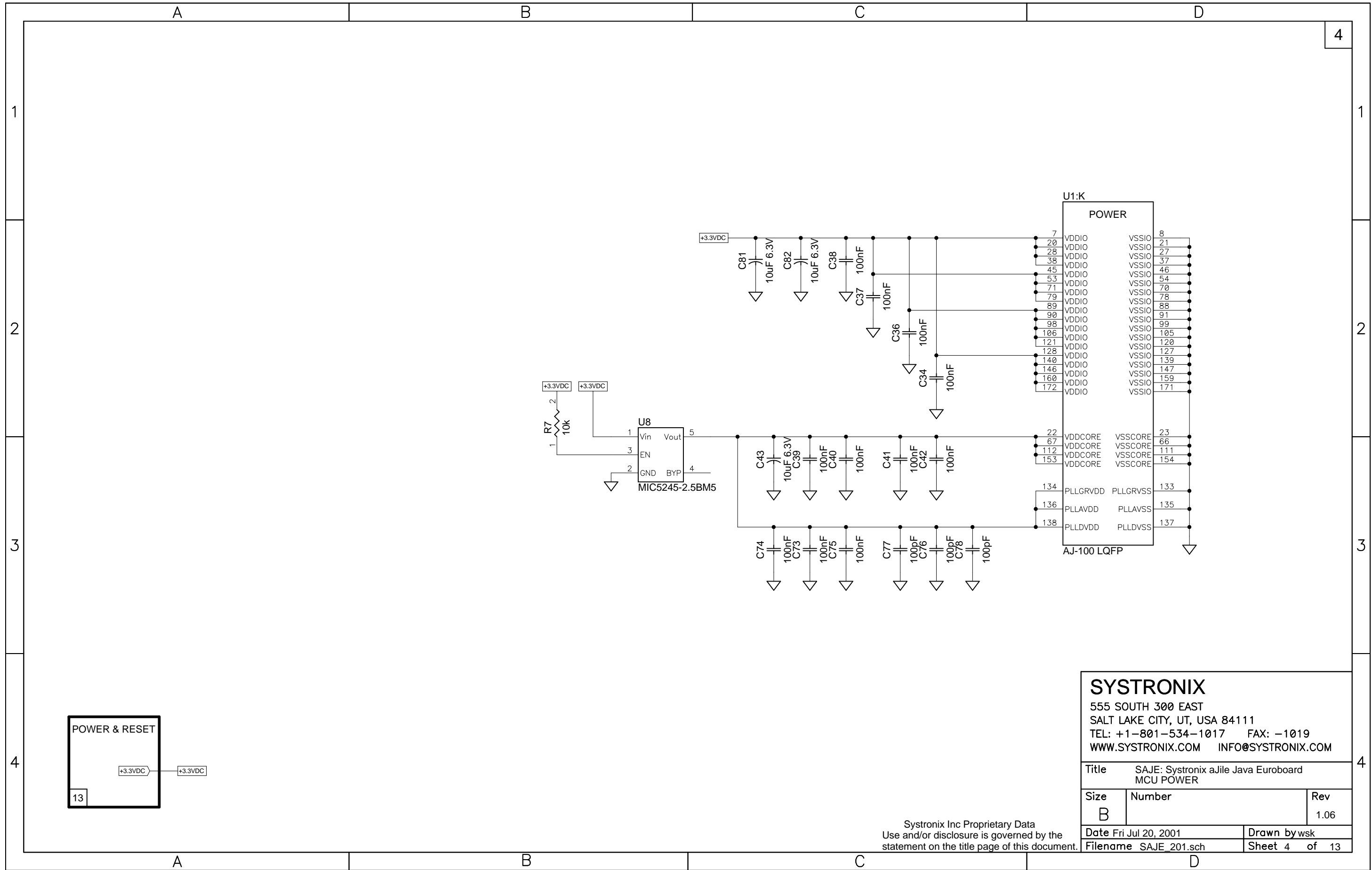
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Title		SAJE: Systronix aJile Java Euroboard MCU: EXTERNAL BUS INTERFACE
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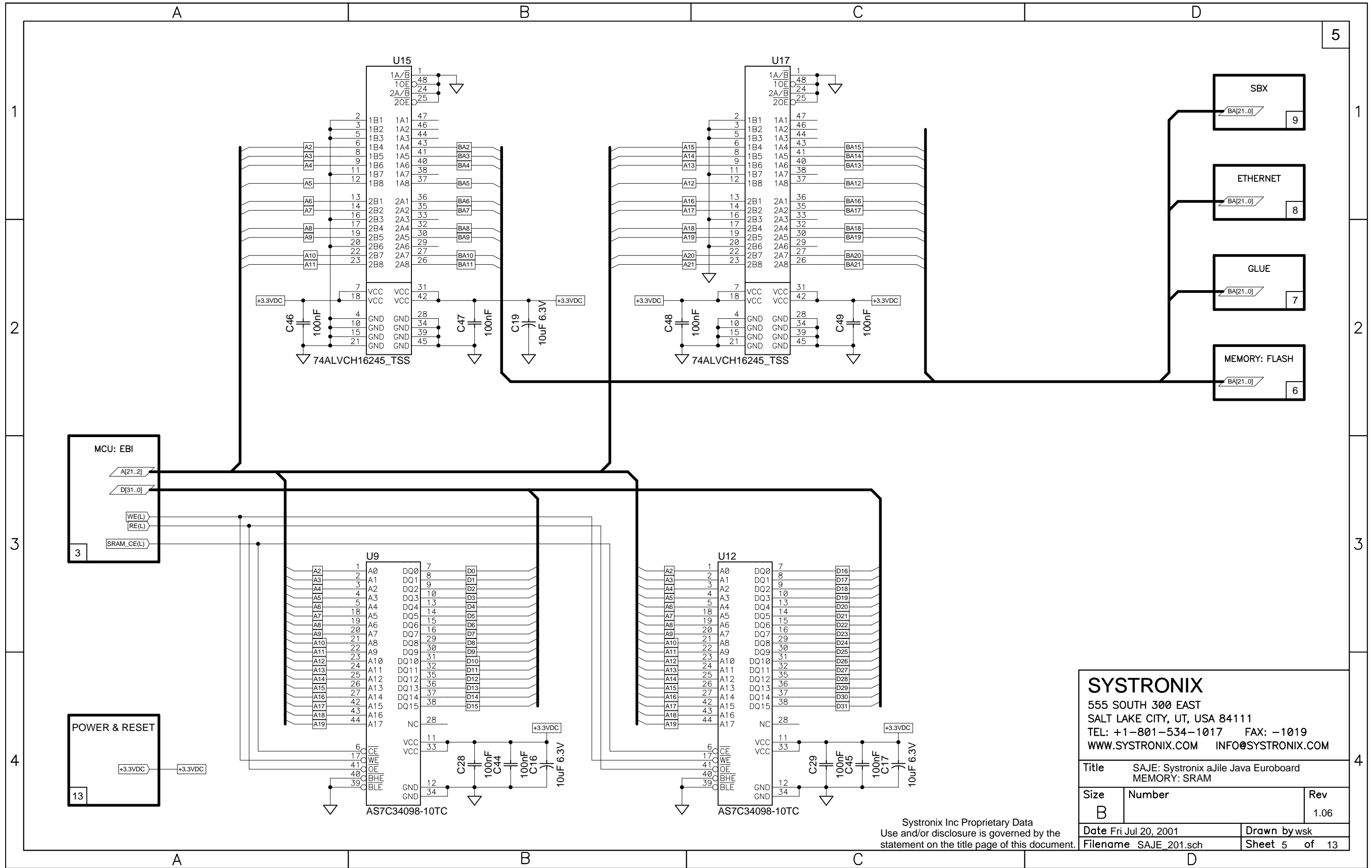
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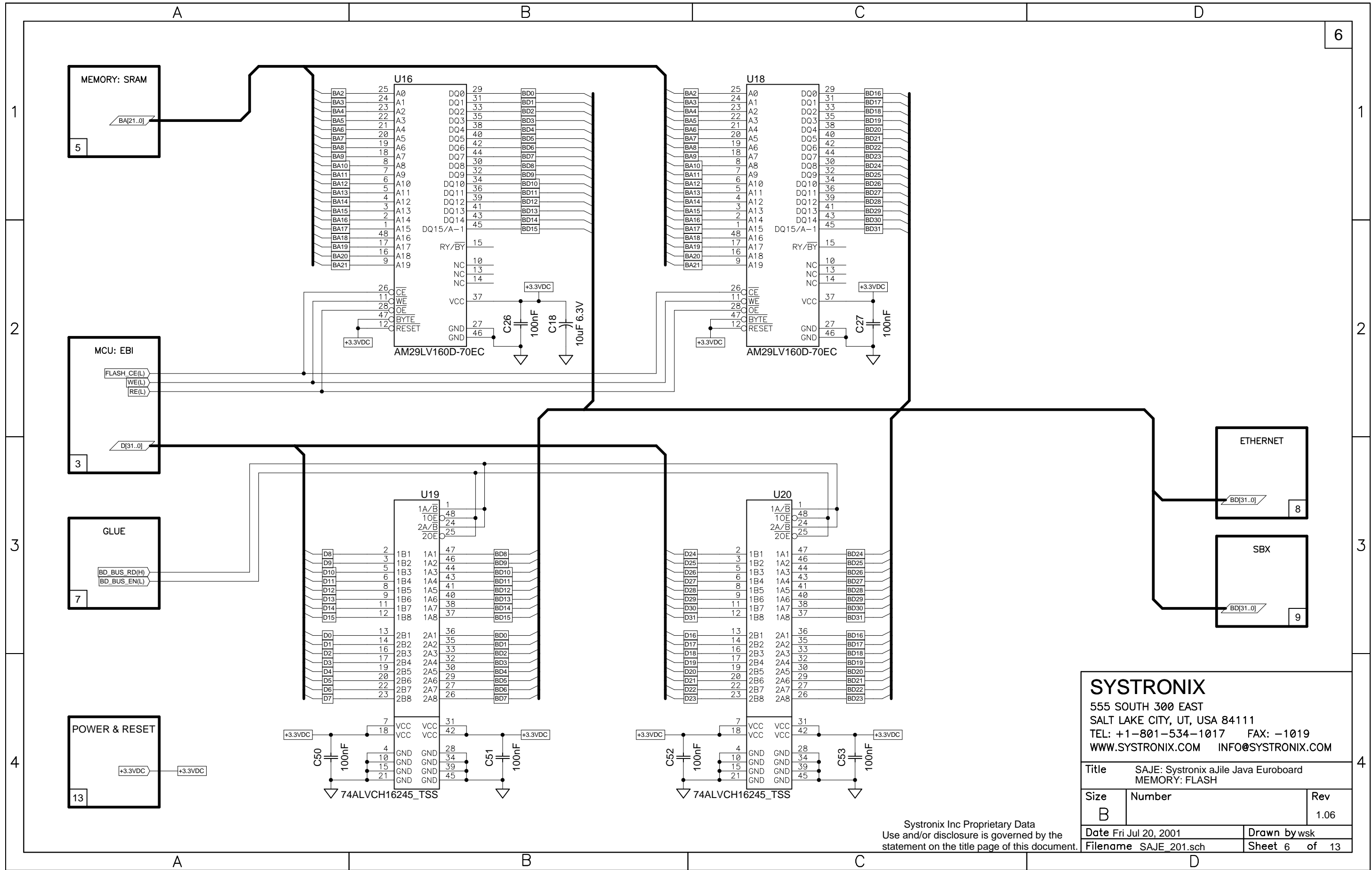
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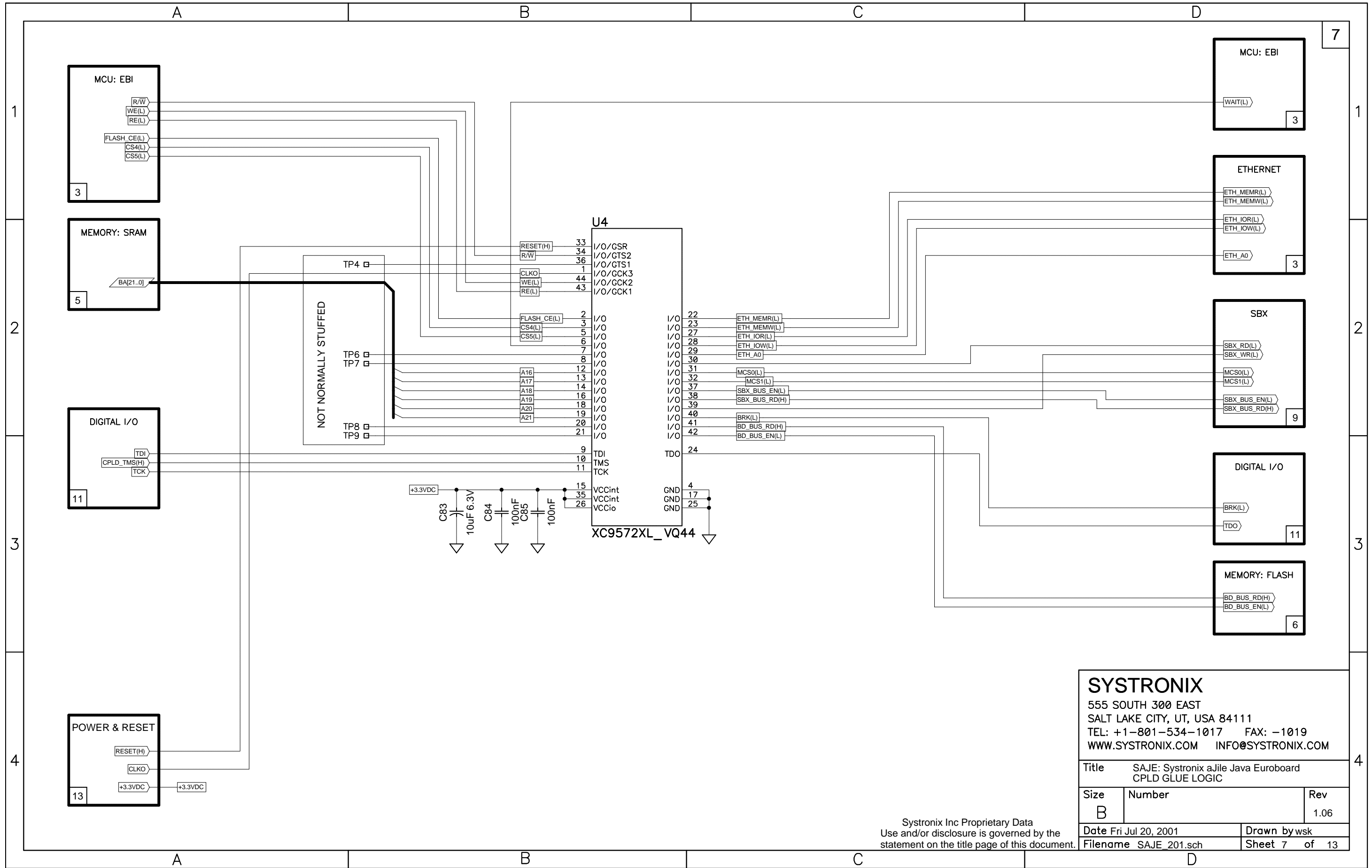
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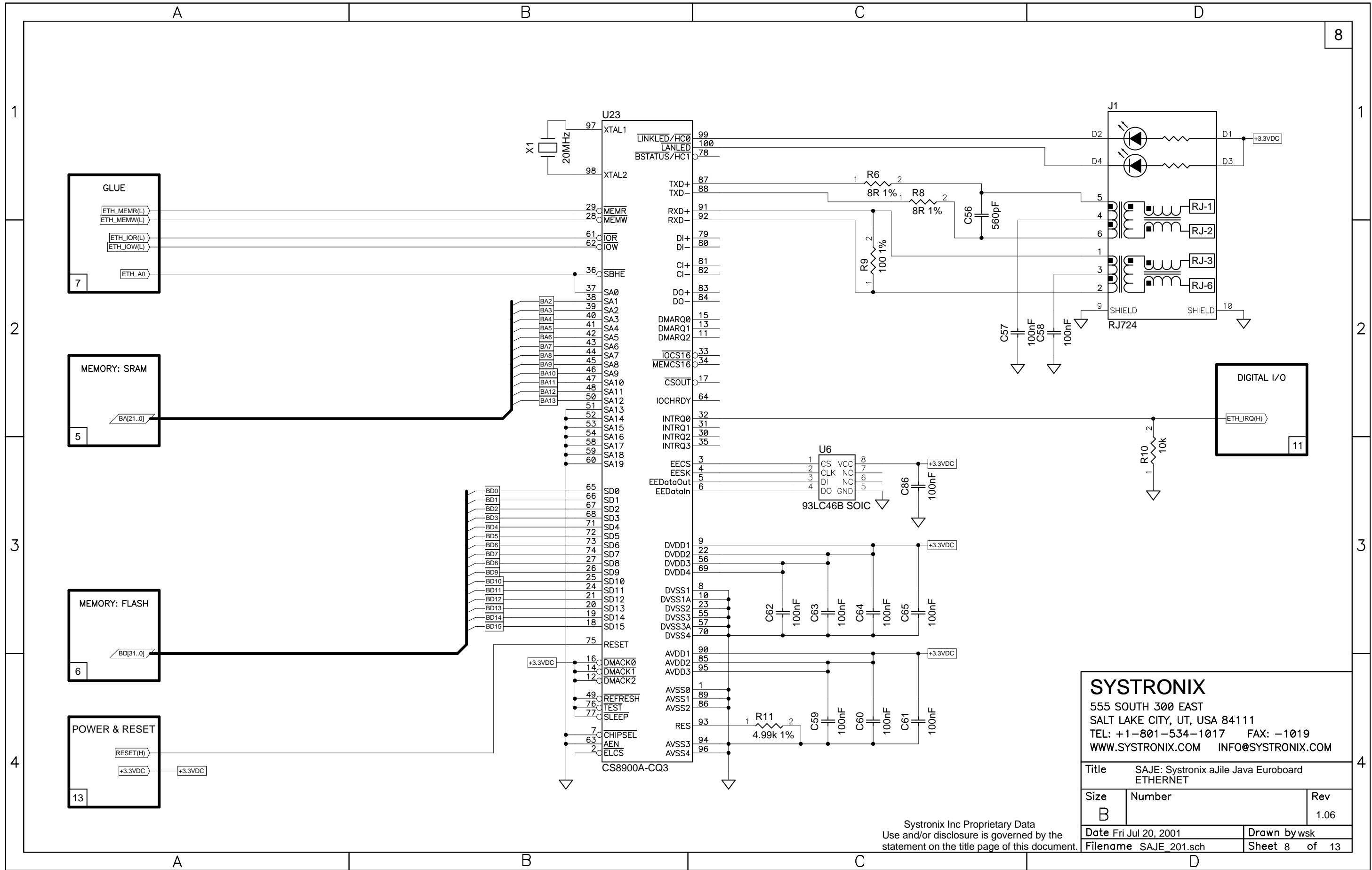
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Title	SAJE: Systronix aJile Java Euroboard MEMORY: FLASH	
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Title SAJE: Systronix aJile Java Euroboard CPLD GLUE LOGIC		
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**GLUE**

ETH\_MEMR(L)  
ETH\_MEMW(L)  
ETH\_IOR(L)  
ETH\_IOW(L)  
ETH\_A0

**MEMORY: SRAM**

BA[21..0]

**MEMORY: FLASH**

BD[31..0]

**POWER & RESET**

RESET(H)  
+3.3VDC

**DIGITAL I/O**

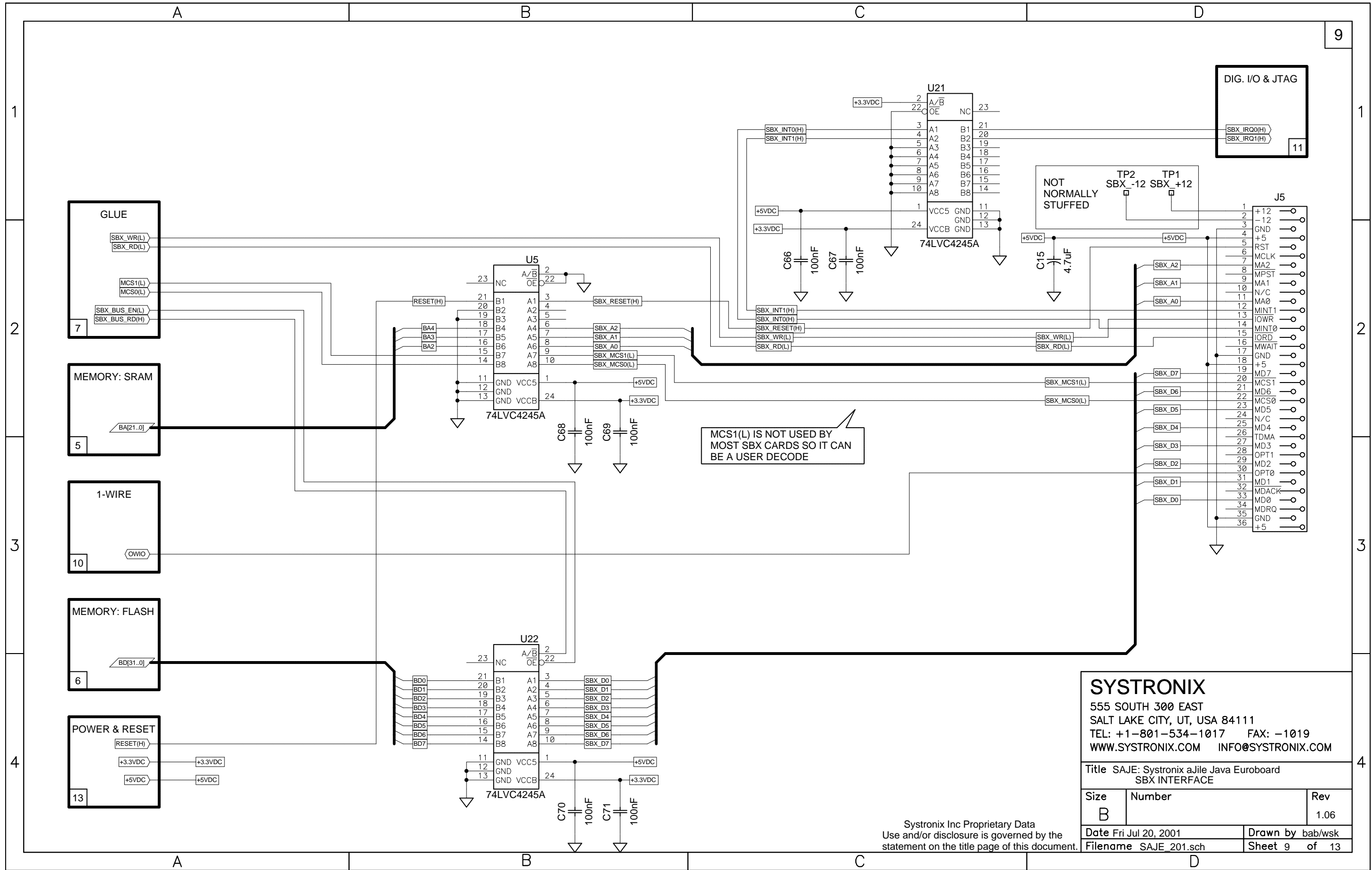
ETH\_IRQ(H)

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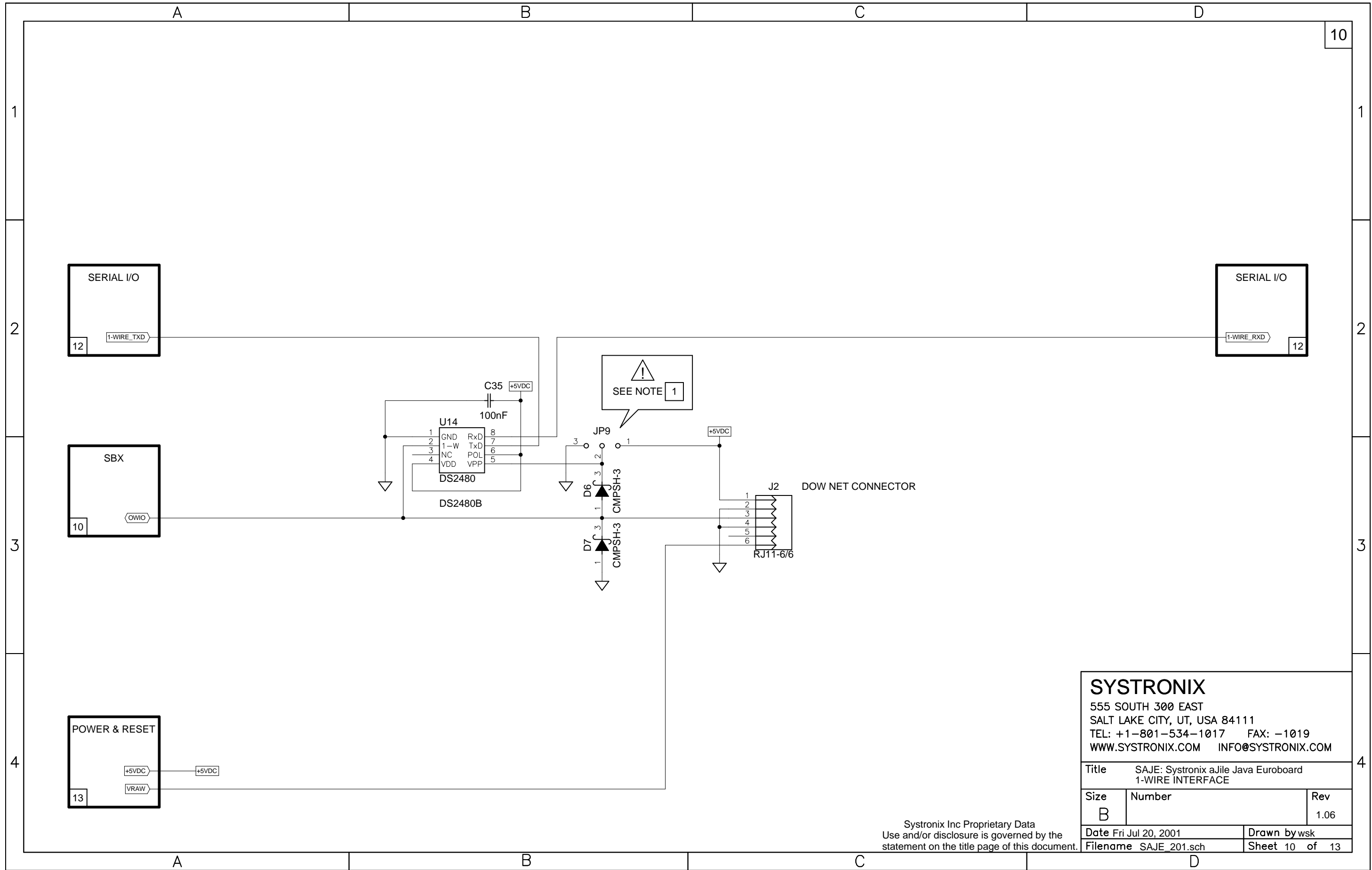


MCS1(L) IS NOT USED BY MOST SBX CARDS SO IT CAN BE A USER DECODE

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Title SAJE: Systronix aJile Java Euroboard SBX INTERFACE		
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1

2

3

4

SERIAL I/O  
12 1-WIRE\_TXD

SERIAL I/O  
12 1-WIRE\_RXD

SBX  
10 OWIO

POWER & RESET  
13 +5VDC VRAW

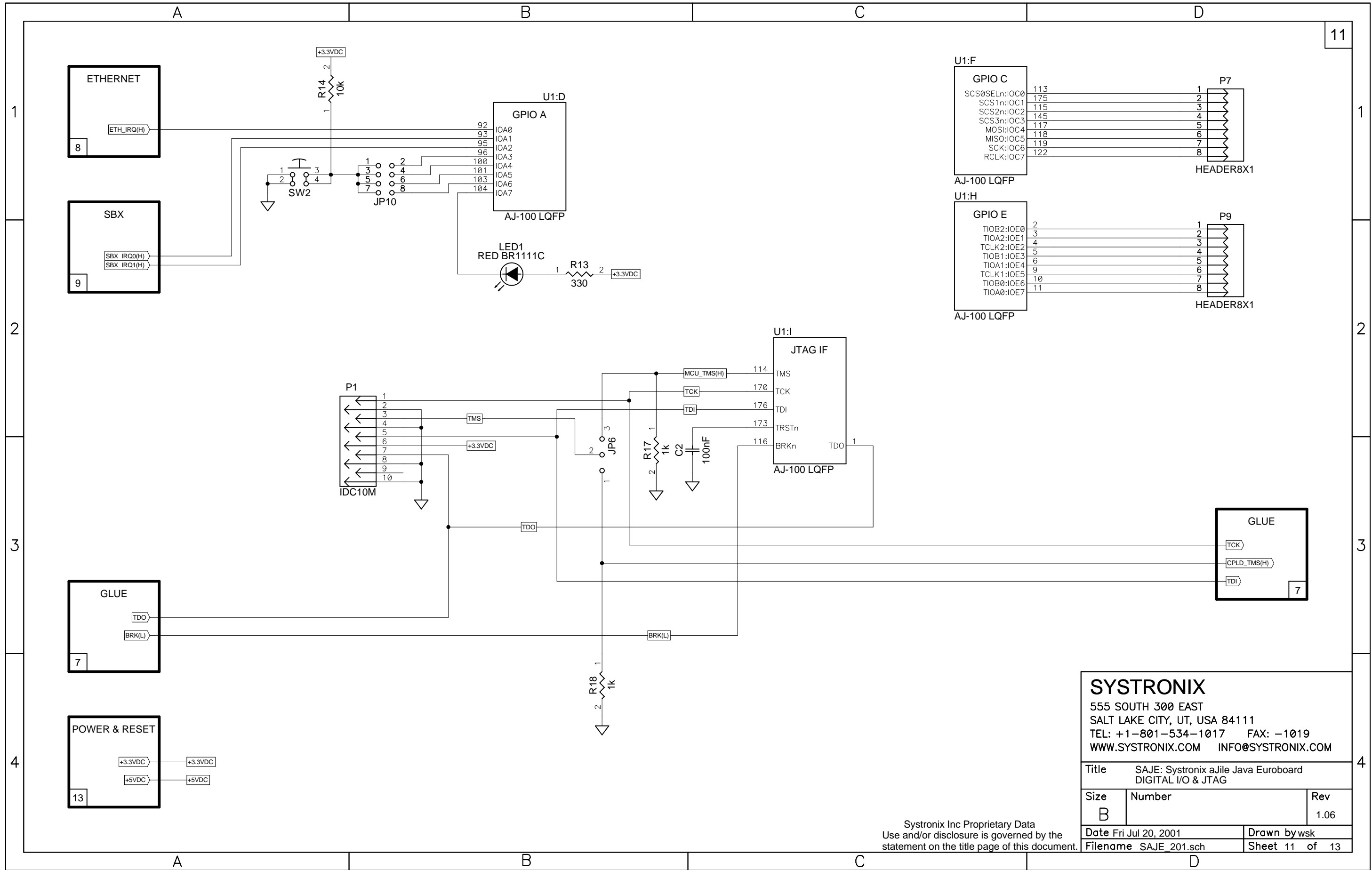
SEE NOTE 1

J2 DOW NET CONNECTOR

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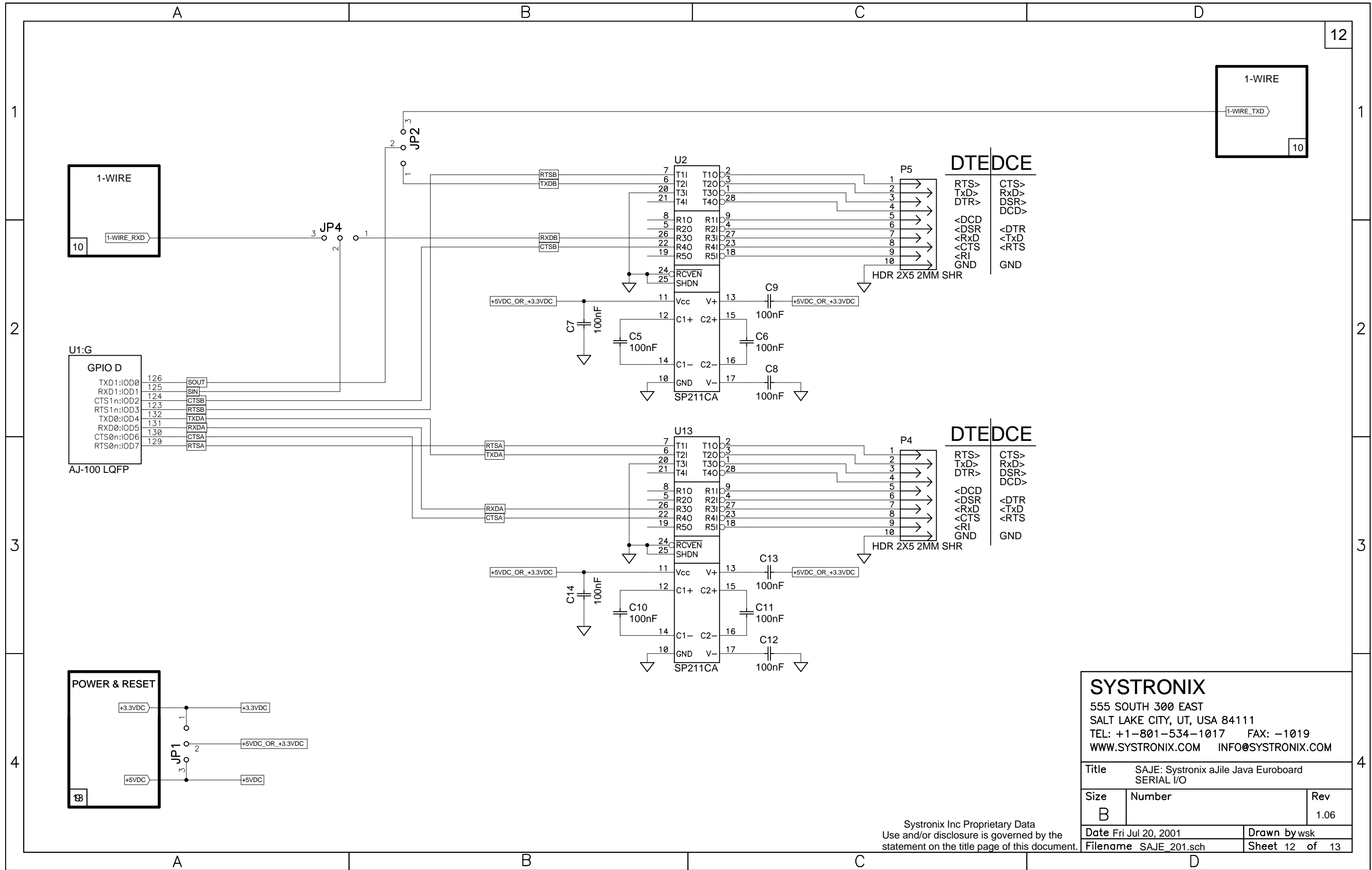
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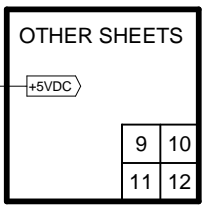
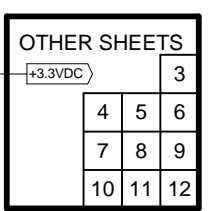
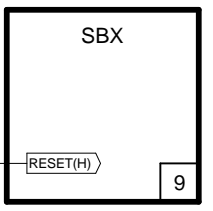
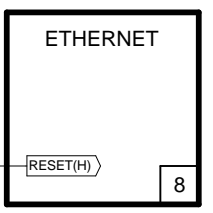
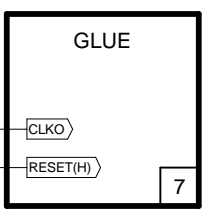
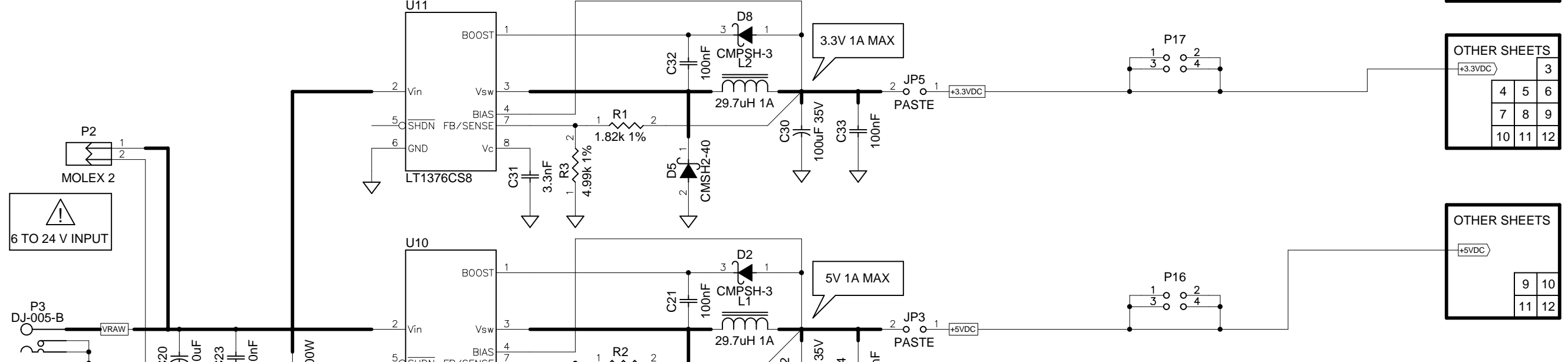
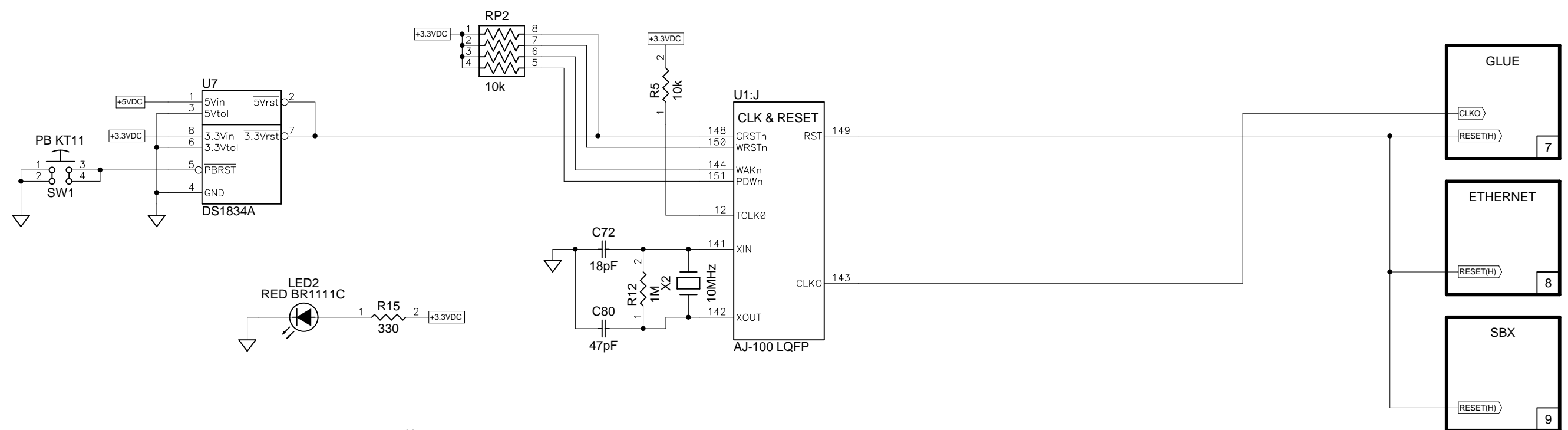
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Title SAJE: Systronix aJile Java Euroboard SERIAL I/O	
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