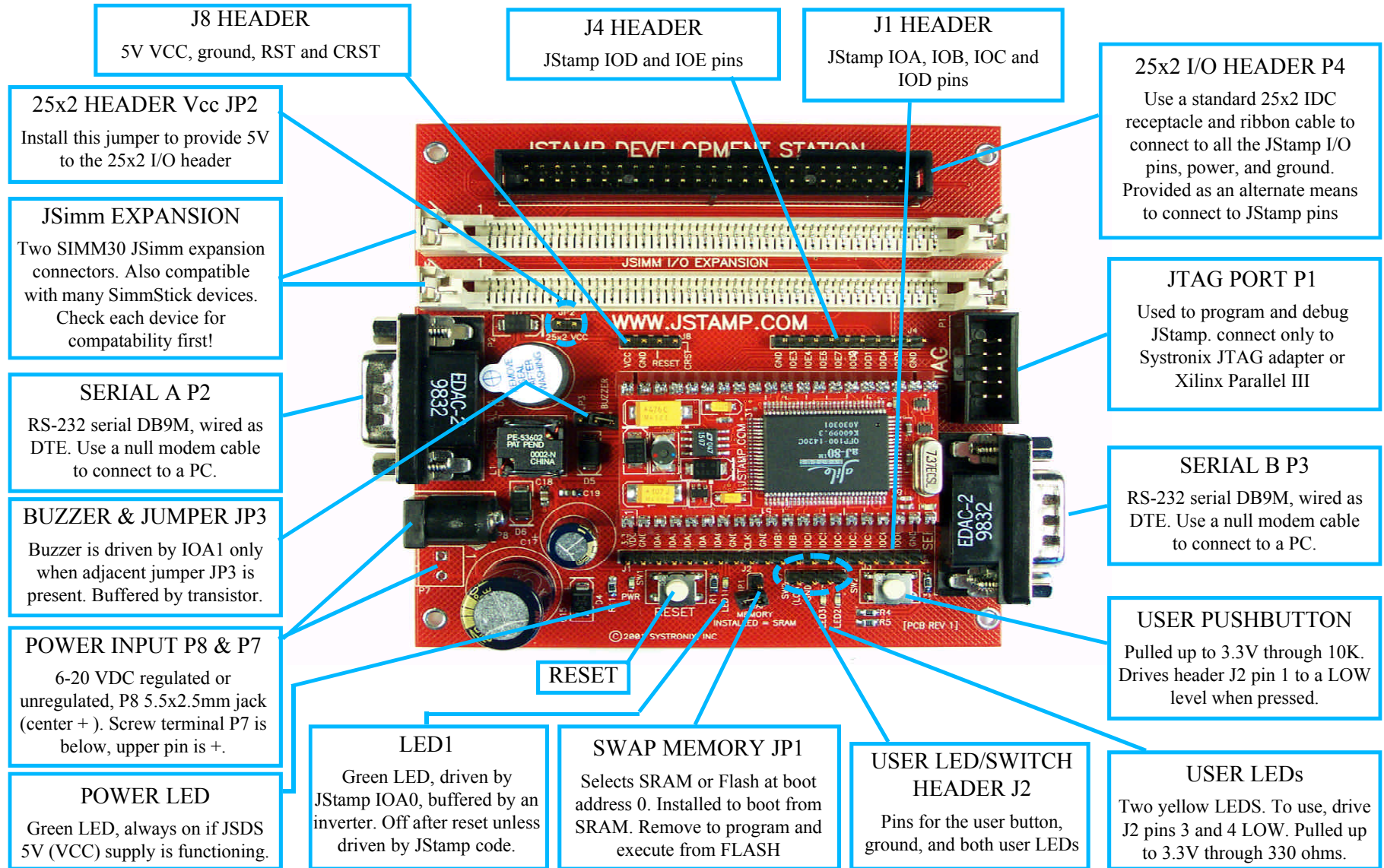


Systronix Rev1 JStamp Development Kit Quick Reference

The most commonly used jumpers and I/O connections are shown here. For more I/O details, please refer to the JStamp and JStamp Development Station schematics and sample code at www.jstamp.com. Tutorials are on line at www.jstampu.com and www.PracticalEmbeddedJava.com

Be sure to check the website before using JStamp for the first time as it may contain essential, last-minute news, documentation, and files.



JStamp™ by SYSTRONIX® www.jstamp.com and www.systronix.com

Quick Reference Notes

Install aJile/Systronix SaJe tools from CDROM - install JemBuilder and Charade from the CDROM provided with your development kit. Check the website at <http://www.jstamp.com> for the latest configuration files, tips or software.

SWAP Memory Jumper - important! - JP1 selects whether JStamp boots up from SRAM (jumper installed) or flash (jumper not installed). You must build (in JemBuilder) for either SRAM or flash, and set the jumper to match. For slightly faster program downloading during development, load into SRAM. (Programs in SRAM are lost when power is removed.) Remove this jumper to enable programming FLASH memory, which persists without system power.

Be sure to build, link, and connect for the correct device - you must specify "JStamp Configuration" (either RAM or Flash, as appropriate) in JemBuilder, and "aJ80" or "JStamp" in Charade in order to correctly build and download programs to JStamp.

JTAG Port - used for loading programs and debugging. Use only the Systronix JTAG adapter and 5x2 100-mil cable, or the Xilinx Parallel III cable. Refer to the schematics for the 5x2 header pinout. Pin 1 is in the lower right corner of the header in the adjacent photograph.

Serial A RS232, a DB9M wired as DTE. A straight-through serial cable will connect to a DCE device such as a modem or LCD. A null modem cable is needed to connect to a PC.

Serial B RS232, a DB9M wired as DTE. A straight-through serial cable will connect to a DCE device such as a modem or LCD. A null modem cable is needed to connect to a PC.

Power Supply is 6-20 volts, DC unregulated or regulated. The input jack is 5.5 x 2.5 mm, center positive or negative. The JStamp Development Station uses an efficient, wide input range switching supply to generate 5 VDC. (JStamp has an onboard 3.3V converter which uses this 5V as its input.) Supply current decreases nearly linearly as supply voltage increases due to the power conversion in the regulator. Recommended power includes the Systronix 1A 12 VDC cube. The regulator can supply at least 500 mA for additional components or expansion cards.

JSimm and SimmStick® Expansion Two SIMM30 connectors are provided. JSimm is compatible with many SimmStick® devices. Check each specific SimmStick® device for compatibility first!

JStamp I/O Headers Header pins (0.025 inches square on 0.100 inch centers) are provided for all JStamp I/O pins. These I/O pins are 3.3V supply, 5V-tolerant, TTL-level compatible. They will drive 5V TTL I/O directly (but will not properly drive 5V CMOS devices). *Some I/O pins have multiple functions - please refer to the JStamp I/O pinout description before selecting pins to connect to your own devices.* Note that the absolute maximum voltage on a 5V tolerant raw JStamp input or I/O pin is 6 VDC. Maximum voltage on a JStamp output pin is 5 VDC. Higher voltages can permanently damage JStamp.

25x2 I/O Header A standard 25x2 polarized header (0.025 inches square posts on 0.100 inch centers) is provided as an alternate means of connecting to JStamp I/O pins. Keep this cable short, and provide your own static or surge protection as needed. Applying an excessive voltage or static to this header can permanently damage JStamp pins. JP2 when present provides 5VDC from the Development Station to the 25x2 header pin 49, through schottky diode D7. The diode prevents power on the 25x2 header pin from driving the JSDS.

Power LED Driven by JStamp's pin IOA0. When IOA0 is high, the JStamp heartbeat LED is lit and so is the Development Station Power LED.

Buzzer Driven by JStamp's pin IOA1. When IOA1 is high, (during and after reset, for example) the buzzer is off. Remove JP3 if you do not want to drive the buzzer.

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JStamp, JSimm, and 25x2 Header Pin Numbering and Description (also see important notes which follow)

JStamp # (note 1,4)	JSimm # (note 5)	25x2 #	Name	I/O (note 6)	Description JSDS=JStamp Development Station
1	none	none	3.3V	I/O	JStamp's power converter provides output of 3.3V @ 100 mA on this pin for your use, when you power JStamp's VRAW input (pin 40). Or you can drive this pin with regulated 3.3 VDC +/- 5%. (JSimm does not have a 3.3V signal, for SimmStick compatibility). (note 7)
can be 40	7	49	5.0V	-	5V can be used as JStamp power input Vraw (pin 40).
2, 8, 10, 20, 21, 30, 39	9	2, 4, 6... 50	GND	-	All even 25x2 header pins are GND (note 3)
3	19	39	IOA4	I/O	24 mA sink/source I/O pin
4	18	41	IOA3	I/O	24 mA sink/source I/O pin
5	17	43	IOA2	I/O	24 mA sink/source I/O pin
6	16	45	IOA1	I/O	24 mA sink/source I/O pin. Drives the JSDS buzzer through an inverter and transistor, if JSDS JP3 is present.
7	15	47	IOA0	I/O	24 mA sink/source I/O pin. Drives the JStamp heartbeat LED through a transistor on JStamp. Also drives the JSDS LED1 through an HCT04 inverter on the JSDS board.
9	6	3	CLK0	0	aJ-80 Clkout signal, a programmable divider output.
11	11	35	IOB5	I/O	8 mA sink/source I/O pin
12	10	37	IOB4	I/O	8 mA sink/source I/O pin
13	22	23	IOC6	I/O	8 mA sink/source I/O pin. Also SPI Transfer Clock.
14	21	25	IOC5/FA1	I/O	8 mA sink/source I/O pin. Also functions as SPI MISO when in SPI master mode and MOSI when a SPI slave. Also used as flash address 1 only when actually programming flash.
15	20	27	IOC4/FA0	I/O	8 mA sink/source I/O pin. Also functions as SPI MOSI when in SPI master mode and MISO when a SPI slave. Also used as flash address 0 only when actually programming flash.
16	3	29	IOC3	I/O	8 mA sink/source I/O pin, or SPI Slave Chip Select 3
17	2	31	IOC1	I/O	8 mA sink/source I/O pin, or SPI Slave Chip Select 1
18	1	33	IOC0	I/O	8 mA sink/source I/O pin, or SPI Slave Chip Select 0 or slave mode select (when JStamp is an SPI slave).
19	29	13	IOD6	I/O	8 mA sink/source I/O pin
22	12	15	IOD5/RXDA	I/O	8 mA sink/source I/O pin, or UARTA RXD (TTL- not RS232 level - note 8)
23	13	17	IOD4/TXDA	I/O	8 mA sink/source I/O pin, or UARTA TXD (TTL- not RS232 level - note 8)
24	28	19	IOD1/RXDB	I/O	8 mA sink/source I/O pin, or UARTB RXD (TTL- not RS232 level - note 8)
25	27	21	IOD0/TXDB	I/O	8 mA sink/source I/O pin, or UARTB TXD (TTL- not RS232 level - note 8)
26	26	5	IOE7	I/O	8 mA sink/source I/O pin
27	25	7	IOE6	I/O	8 mA sink/source I/O pin
28	24	9	IOE4	I/O	8 mA sink/source I/O pin
29	23	11	IOE3	I/O	8 mA sink/source I/O pin
31	none	none	SWAP_MEM(L)	I	Leave floating high to select and/or program flash memory at memory location 0 (this is the typical state of this pin). Pull this pin low to place SRAM at location 0 (normally used only in development).
32	none	none	JTAG_TDO	0	JTAG Test Data Output (note 2)
33	none	none	JTAG_TDI	I	JTAG Test Data Input (note 2)
34	none	none	JTAG_TMS	I	JTAG Test Mode Select (note 2)
35	none	none	JTAG_TCK	I	JTAG Test Clock input (note 2)
36	8	1	CRST(L)	I/O	Open-drain reset to/from JStamp. Use this signal to reset JStamp from external logic or to reset your external logic when JStamp resets.
37	5, 14, 30	none	N/C	-	Do not connect to this pin. May be used in a future JStamp version.
38	none	none	RESET_PB(L)	I	Input to JStamp from a reset pushbutton. Circuitry on JStamp debounces this. Use this signal to reset JStamp from a switch.
40	4	none	VRAW	-	Power JStamp with 5-14 VDC on this pin if you do not provide regulated 3.3 VDC on JStamp pin 1.

Pinout Notes

Note 1: JStamp I/O Pin Voltages and Logic Thresholds - JStamp GPIO pins are 3.3V max Voh, compatible with TTL levels, and are 5V I/O tolerant. They interface with no additional circuitry to 3.3V and 5V TTL-level devices. They will not drive 5V CMOS outputs directly.

Note 2: JTAG pins must be connected only to a Systronix JTAG adapter or Xilinx Parallel III programming adapter. Any other connection voids your warranty and may damage JStamp.

Note 3: Ground - JStamp grounds are all connected together, so in a minimal system you only need to connect at least one to your system.

Note 4: GPIO Pin Function - Each GPIO pin may be individually configured as input or an output. Every GPIO pin may also be configured to generate a CPU interrupt. Interrupt flexibility is provided by allowing interrupts to be triggered on a rising edge, falling edge, either edge, high level, or low level. To minimize pin-count most of the GPIO signals are shared with other I/O signals of the aJ-80. On a reset the shared signals are configured as GPIO inputs. Operation of the shared signals is controlled with the I/O configuration registers.

Note 5: JSimm pins - JStamp uses some GPIO pins for specific purposes when using the JSimm interface.

Note 6: I/O Direction is from the viewpoint of JStamp. I.e., an input is an input to JStamp.

Note 7: JStamp power can be either regulated 3.3 VDC +/- 5%, or unregulated 4.5-14 VDC +/- 5%. If you power JStamp's VRAW input (pin 40) then JStamp's 3.3V I/O (pin 1) provides output of 3.3V @ 100 mA for your use. If you provide regulated 3.3 VDC on pin 1, do not connect VRAW. *Under no circumstances should power be applied to both Pin 1 and Pin 40.* When JStamp is plugged into the Development Station, it receives 5VDC on pin 40.

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JStamp Documentation and Resources

aJ-80 and aJ-100 - both aJile controllers share the same 32-bit CMOS core and differ only in pinout (the aJ-100 is a larger package so brings out more pins). The aJ-80 has an 8-bit external data bus - the aJ-100 has 32-bits. They share the same technical reference, Java edition and profile support, and so forth.

AJ-100 Reference Manual - available online at <http://www.ajile.com/aj100.htm> as a PDF document. This is the definitive source for information about inner workings of the aJile controllers.

On-line Support Groups: there is a JStamp Yahoo user group at <http://groups.yahoo.com/group/jstamp> as well as other third party support and information groups. Links to those may be found at <http://www.jstamp.com>

Java, J2ME, CLDC, and RealTime Java Information: J2ME and CLDC information and packages are available online from Sun at <http://www.sun.com/software/communitysource/j2me/cldc/download.html> and there are also links to Java resources at <http://www.jstampu.com>

JStamp in Robotics: www.jcx.systronix.com

JCX is a JStamp-based platform with LEGO®-compatible inputs and outputs, (also usable with other common robotic sensors and actuators). App notes are on line here - for example, driving a sonar rangefinder from JStamp.

Tutorial & Examples, Educational Use: www.jstampu.com

An ongoing tutorial and sample programs are available on our web site at www.jstampu.com. There are also links to use of JStamp and related products in education, particularly university and college programs.

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