

JSimm.JStamp

1

SCH REV	PCB REV	DATE	BY	DESCRIPTION	SCH REV	PCB REV	DATE	BY	DESCRIPTION
0.0		01 MAY 17	wsk	START					
1.00	1.00	01 MAY 24	wsk	PCB REV 1 DONE.					
1.01		01 MAY 31	wsk	Sheet 1: Added Note 3;					
1.10		01 JUN 05	wsk	Sheet 3: Changed P1 to 100 mil header; Sheet 4: Renamed nets RXDA, RXDB, TXDA, TXDB;					
2.00	2.00	01 OCT 09	wsk	Sheet 3: Deleted connections to sheet 5 (CAN I/O); Sheet 5: Deleted;					
2.01		01 NOV 14	wsk	Sheet 2: Deleted Note 1, Note 2, Note 3; Sheet 3: Changed signal name from IOE5 to IOE6, Added LED1, LED2, P5, R1, R3, U4; Connected M2-40 to VRAW; Sheet 4: Deleted 1-Wire support: C13, D1, D2, JP4, JP9, P5, R1, R6, R7, U2, U4, U7; Changed U3 to SP312A, RP2 to 100;					
3.00	3.00	03 JUN 20	wsk	Sheet 3: Added TP1; Changed values of C1 & C7; Sheet 4: Inverted and labeled signal at U3 pin 25;					
3.10	3.10	04 MAR 01	wsk	Sheet 3: Added TP1; Corrected LED1 & LED2 connections;					

TABLE OF CONTENTS

SHEET	TITLE
1	REVISIONS
2	NOTES
3	JSimm INTERFACE
4	SERIAL I/O

TO DO:

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Title JSimm.JStamp REVISIONS	
Size B	Rev 3.00
Date Mon Mar 01, 2004	Drawn by wsk
Filename JSimm_JStamp_310.sch	Sheet 1 of 4

A

B

C

D

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JP1	INSTALLED	Routes JStamp CLKO to JSimm Bus
JP2	INSTALLED OPEN	JStamp boots from SRAM JStamp boots from FLASH
JP3	1-2 2-3 BOTH OPEN	com2 IrDA at P2 com2 RS-232 serial at P4 com2 TTL at the JSimm connector
JP4	INSTALLED	Routes JStamp +3.3VDC to/from JSimm Bus
JP5	INSTALLED OPEN	com1 RS-232 serial at P3 com1 TTL at the JSimm connector

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Title JSimm.JStamp NOTES		
Size B	Number	Rev 3.00
Date Mon Mar 01, 2004	Drawn by wsk	
Filename JSimm_JStamp_310.sch	Sheet 2 of 4	

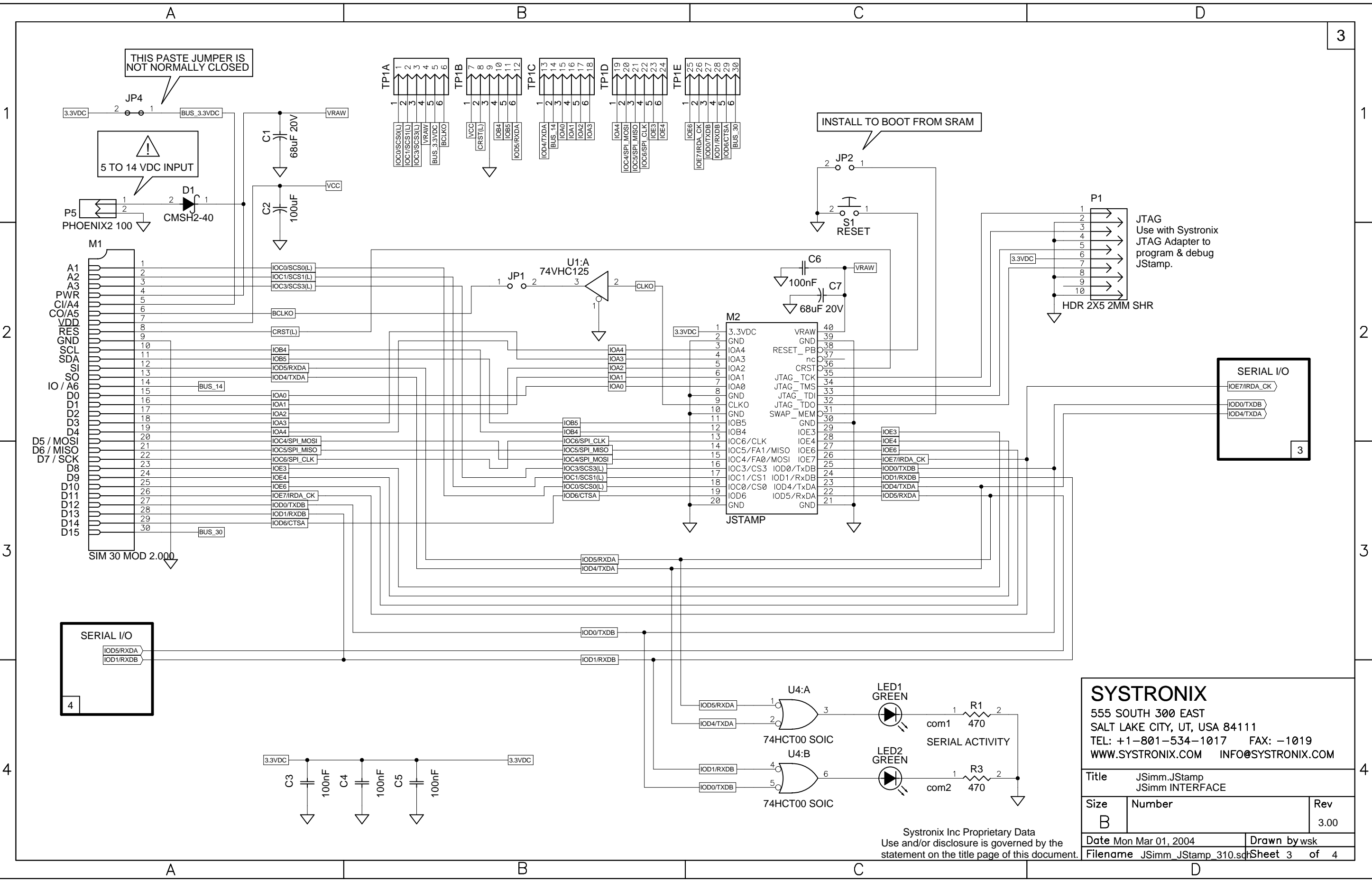
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A

B

C

D



3

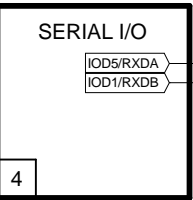
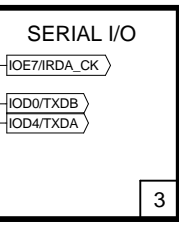
1

2

3

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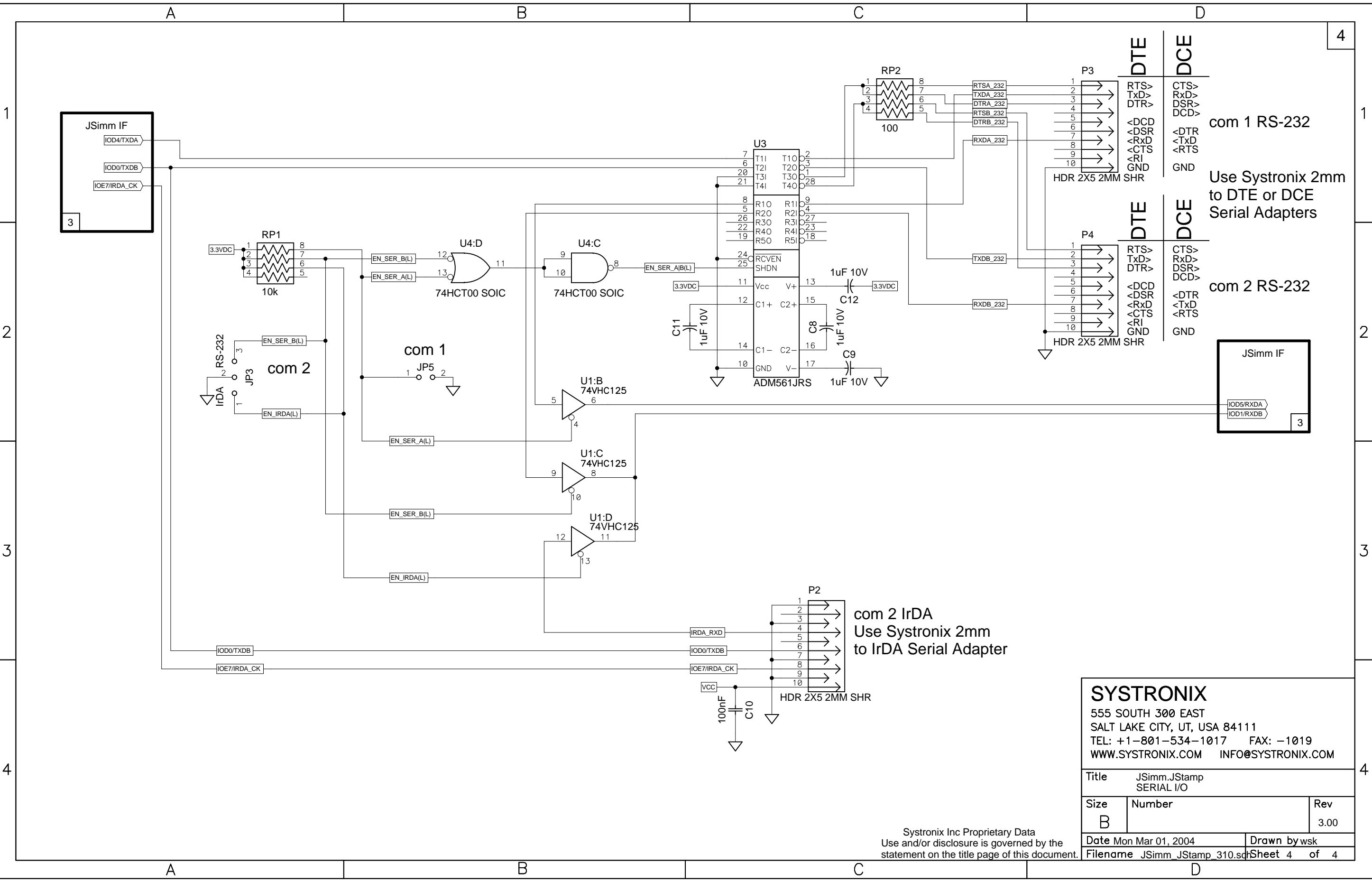
JTAG
Use with Systronix
JTAG Adapter to
program & debug
JStamp.



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Title JSimm.JStamp JSimm INTERFACE		Rev 3.00
Size B	Number	
Date Mon Mar 01, 2004	Drawn by wsk	
Filename JSimm_JStamp_310.sch	Sheet 3 of 4	

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com 1 RS-232
Use Systronix 2mm to DTE or DCE Serial Adapters

com 2 RS-232

com 2 IrDA
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Filename JSimm_JStamp_310.sch	Sheet 4 of 4	

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